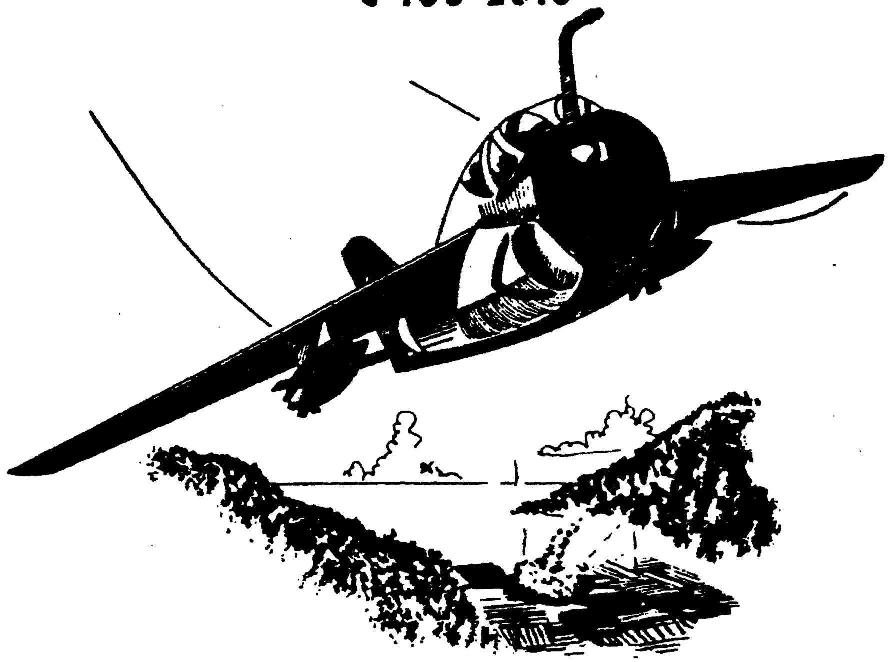
Prepared for

AVIONICS TECHNICIAN COURSE, CLASS A

C-100-2013



MODULE 5-5

SYNCHRONIZER - DISPLAY INDICATOR CIRCUIT ANALYSIS

CNTT-M1206 (REV. 8-84)

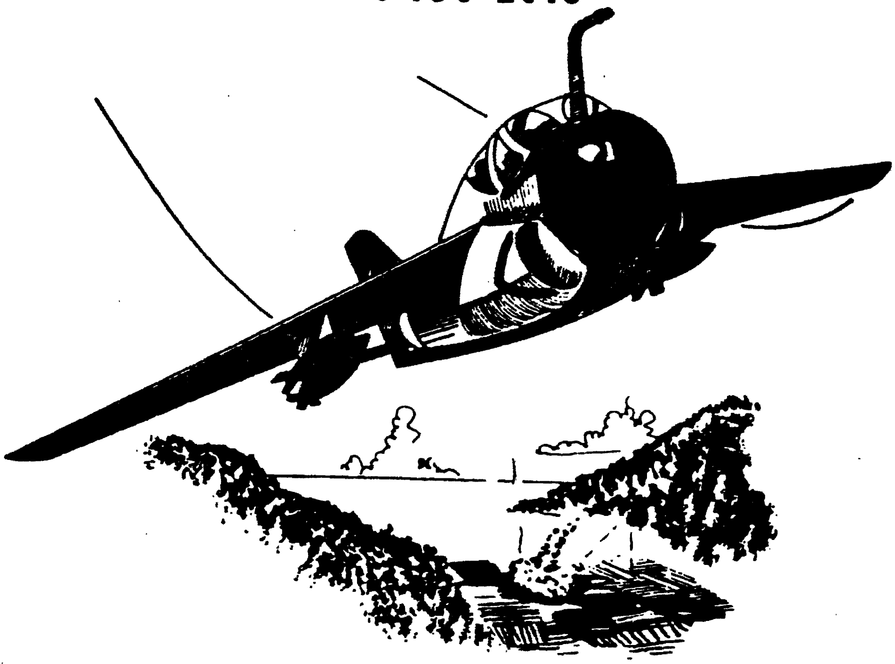
Prepared by

Naval Air Technical Training Center
Naval Air Station Memphis,
Millington, Tennessee

Prepared for

AVIONICS TECHNICIAN COURSE, CLASS A1

C-100-2013



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UNIT 5

MODULE 5

LESSON TOPIC 1

UNIJUNCTION TRIGGER OSCILLATOR

OVERVIEW

LESSON TOPIC 5-5-1

UNIJUNCTION TRIGGER OSCILLATOR

In this lesson topic the triggered unijunction oscillator will be taught in detail. The circuit configuration and the operation of the circuit components in relation to the application of triggered unijunction oscillators within an airborne search radar system will be explained.

The learning objectives for this lesson topic are as follows:

1. Select, from a list, the symbol that represents a unijunction transistor.

2. Select from a list, the components of the unijunction oscillator that determines the shape of the output trigger.

3. Select from a list, two statements that describe the circuit application of the unijunction trigger oscillator.

4. Select from a list, the statement that describes, in relation to output waveform, the circuit function of Q3 in the unijunction trigger oscillator circuit.

5. Select from a list, two statements that describe the circuit functions of L1 and R22 in the unijunction trigger oscillator.

6. Select, from a list, two statements that describe, in relation to the output waveform, the circuit functions of C11, R20, and R17 in the unijunction trigger oscillator circuit.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-1

UNIJUNCTION TRIGGER OSCILLATOR

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job program in Job Program Booklet.
2. Student response sheets.
    a. Job Data sheet.
    b. Answer sheet for use with test.
    c. Programmed instruction response sheets.

ENRICHMENT MATERIALS:

1. Airborne Search Radar Training Device (15A21) Maintenance Instruction Manual.
2. Fundamentals of Electronics, E. Norman Lerch, 2nd edition, pp. 120, 712, 713.

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objectives at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

UNIJUNCTION TRIGGER OSCILLATOR

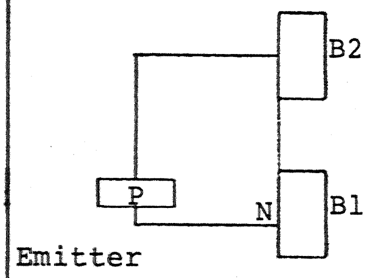
INTRODUCTION

In any radar system, timing is essential to the correct operation of the system. To achieve this exact timing, it is necessary to have a stable reference oscillator. Many different types of reference oscillators are employed in radar systems such as: blocking oscillators, multivibrators, crystal controlled oscillators, and other types of relaxation oscillators.

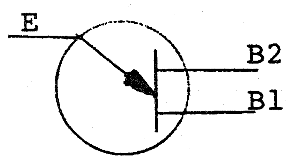
The airborne search radar system trainer employes a unijunction trigger oscillator. This oscillator is located on the resolver driver circuit card (A3A1).

P.I.

1. The unijunction transistor is a specially designed semiconductor device. The double-based diode or UNIJUNCTION TRANSISTOR is constructed with a small rod of P-type material extending into a block of N-type material which serves as a P-N junction. Two bases are welded to the block of N-type material without forming new junctions. Refer to (a) in Figure 1. The schematic symbol for the unijunction transistor (b) in figure 1, shows the emitter (E) and the two base connections (B1, B2).



(a)



(b)

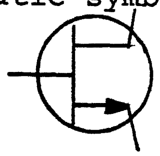
FIGURE 1

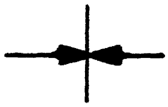
P.I.

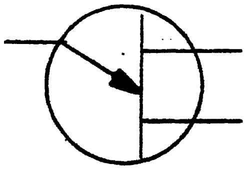
Module 5-5
Lesson Topic 5-5-1

1. (Continued)

The unijunction transistor is a specially constructed semi-conductor device and the schematic symbol is

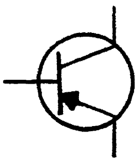
(a) 

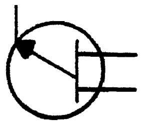
(b) 

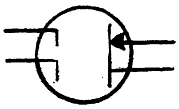
(c) 

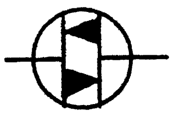
c.

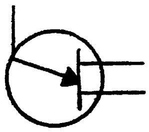
2. Select two schematic symbols for unijunction transistors.

a. 

b. 

c. 

d. 

e. 

b,

e.

3.

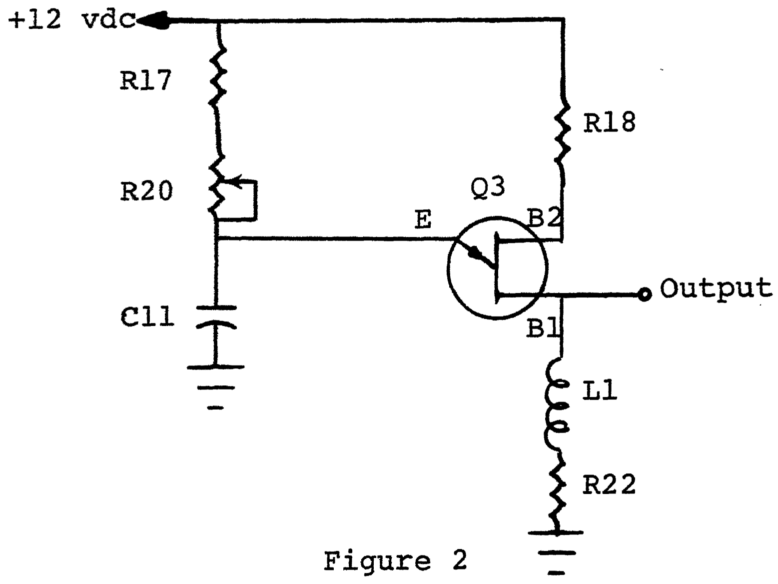


Figure 2

Figure 2 illustrates the unijunction trigger oscillator as it is configured on the Resolver Driver Card (A3A1) of the radar's synchronizer. When power is applied to the circuit, C11 begins charging towards +12vdc through R17 and R20. Q3 requires a bias voltage of +8vdc on the emitter to conduct. When the charge on C11 reaches +8vdc, Q3 becomes forward biased and conducts, providing a discharge path for C11. The discharge path is through ground, R22, L1, and the B1-E junction of

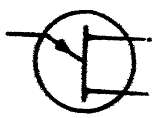
P.I.	
	3. (continued) Q3. The combination of <u>C11</u>, <u>L1</u>, <u>R22</u> <u>shapes the output pulse</u> into a high amplitude, narrow pulse of voltage. When C11 is fully discharged, Q3 cuts off and C11 starts charging again, beginning another cycle of operation. In the unijunction trigger oscillator shown in figure 2, the components that determine the ________ of the output pulse are C11, L1, and R22.
shape	4. Refer to figure 2. The components that determine the shape of the output pulse are a. R18, L1, R22. b. C11, R17, R20. c. C11, Q3, R18. d. C11, L1, R22.

P.I.

d.

5. The design of a unijunction transistor is a small rod of P-type material extending into a block of N-type material and two base leads welded to the block. The base contacts do not form PN junctions.

Draw the schematic symbol of a unijunction transistor.



6. The characteristics of the output pulse from the unijunction oscillator make it especially suitable for use as a timing pulse.

The output of the 1kHz trigger oscillator (unijunction oscillator) serves two functions in the airborne search radar trainer.

First, during standby operation of the radar the clock trigger is routed through the modulator to the sweep gate generator within the synchronizer unit to initiate

P.I.

6. (continued)

the development of the positive and negative sweep gates.

Second, during transmit operation, the clock trigger is applied to the Pulsed Switching device (SCR) within the modulator. This initiates the firing of the transmitter. The shape of the output pulse is shown in figure 3.

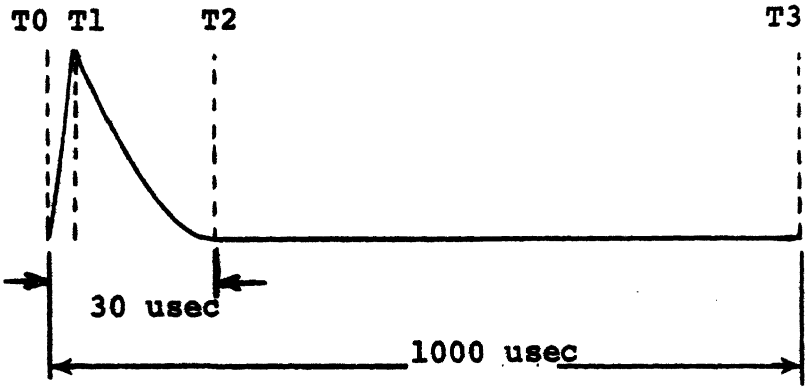
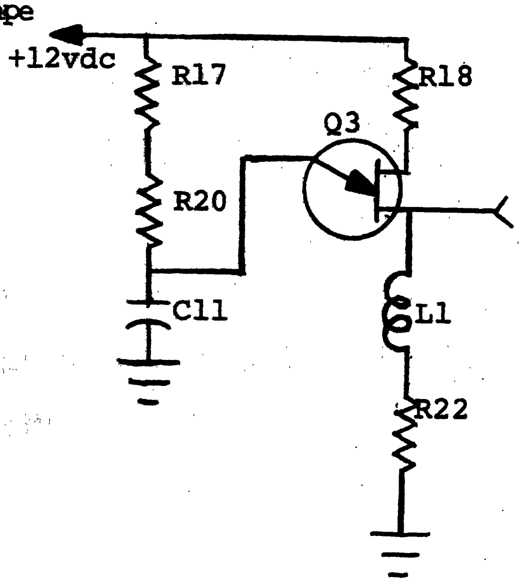


Figure 3

Notice that the leading edge is nearly vertical. This is a necessary requirement to ensure the rapid switching action of the SCR and sweep gate generator.

P.I.	
	6. (Continued) Two applications of the output pulse from the unijunction oscillator are to trigger the __________ ______________ generator during standby operation and trigger the pulsed ________ _____(SCR) during transmit operation.
sweep gate switching device	7. The output of the unijunction trigger oscillator is used in the radar system to trigger the _________ __________ ______( ) during transmit operation and the _________ ________ __________ during standby operation.
pulsed switching device (SCR) sweep gate generator	8. In the unijunction oscillator shown below, C11, L1, and R22 determine the output pulse ______________ of the circuit. amplitude/shape

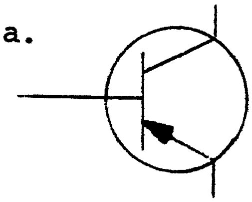


P.I.

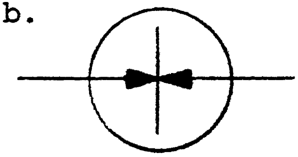
shape

9. Which symbol below represents a unijunction transistor?

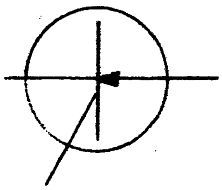
a.



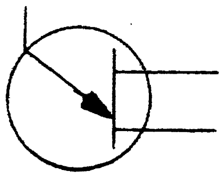
b.



c.



d.



P.I.		Module 5-5 Lesson Topic 5-5-1
d.	10.	

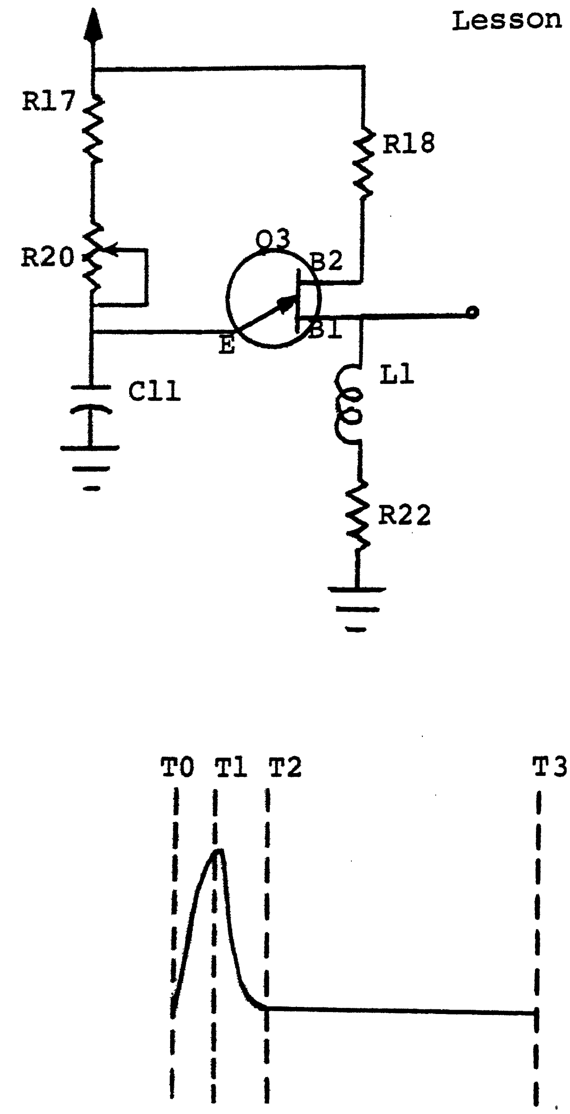


FIGURE 4

The unijunction transistor, Q3, in figure 4 functions as a switch to provide a discharge path for capacitor C11 in the emitter circuit. When Q3 conducts, C11 discharges

P.I.

10. (Continued)

rapidly through R22, L1, and B1-E of Q3, producing the positive pulse from time zero (T0) to time two (T2) at the output. At time two (T2), C11 has completed its discharge and Q3 cuts off, and C11 charges back up, T2 to T3.

In the unijunction oscillator in figure 4, Q3 acts as a ____________________ to provide a discharge path for C11 from T0 to T2.

P.I.

switch

11. Refer to figure 4. The conduction of Q3 provides a

a. charge path for C11 from T0 to T2.

b. discharge path for L1 from T0 to T1.

c. discharge path for C11 from T0 to T2.

d. charge path for L1 from T0 to T1.

c.

12. Two applications of the unijunction trigger oscillator in the radar are

a. to __________ the pulsed switching device (SCR) during transmit operation.

b. to trigger the __________ __________ __________ during standby operation.

a. trigger.

b. sweep gate generator

13. Which of the components in figure 4 determine the shape of the output pulse?

a. R17, R20, C11.

b. L1, R22, C11.

c. R18, Q3, C11.

d. L1, R18, R22.

P.I.	
b.	14. Inductor L1 and resistor R22 make up the load for the unijunction transistor oscillator. The output pulse produced by the unijunction transistor oscillator is developed across the reactance of L1 and the dc resistance of R22 between T0 and T2. The inductor also provides some sharpening of the output pulse. The reactance of L1 and the dc resistance of R22 in conjunction with C11, also determine the discharge time of C11. Between T0 and T2, the output of the unijunction trigger oscillator is developed across _____________ and _________, these components also determine the ___________ time of C11.
L1 R22 discharge	15. The output of the unijunction trigger oscillator is a narrow, high amplitude pulse of voltage and is developed across ___________ and ___________ and the discharge time of ___________ is determined by ___________ and _______________.

P.I.	
L1 R22 C11 L1 R22	16. When Q3 switches "ON", it provides a ________________ path for C11 through L1 and R22. charge/discharge
discharge	17. Which two statements below describe the application of the unijunction trigger oscillator? a. Used to trigger the pulsed switching device in the modulator during transmit operation. b. Used to fire the transmitter during radar operation. c. Provides clock pulses to trigger the sweep gate generator during standby operation. d. Used to synchronize the master oscillator in the synchronizer unit.
a, c.	18. Refer to figure 4. The path for the charging of C11 is through R20 and R17 to the power supply voltage (+12 vdc). R20 is variable to provide a means for adjusting the charge time. When the charge on the emitter

P.I.

18. (Continued)

side of C11 is positive enough it will cause the unijunction transistor, Q3, to conduct. In figure 5, the emitter waveform of Q3 is shown in synchrogram with the output. It can be easily seen that C11 <u>charges</u> during the <u>rest time</u> of the output, or from <u>T2</u> to <u>T3</u>, and discharges from T0 to T2, developing the output.

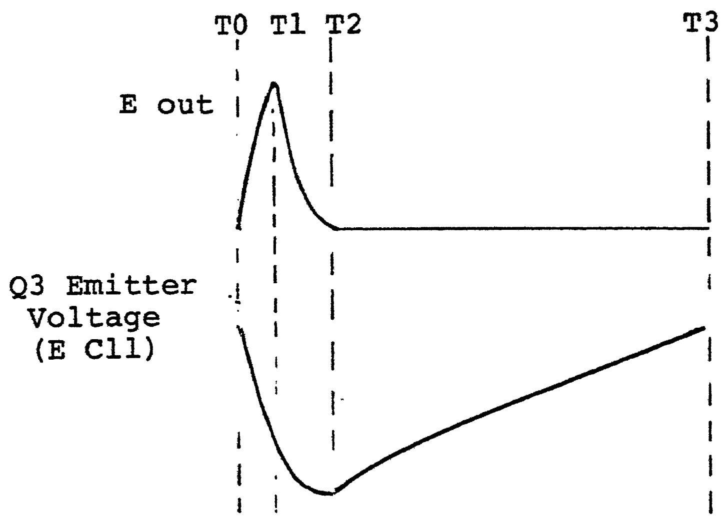


Figure 5

18. (Continued)

The rest time of the output waveform is determined by the time required for C11 to charge through R17 and R20, to a high enough voltage to trigger Q3 into conduction.

The RC time of the charge path of C11 is determined by R17 and R20 and determines the ____________ ____________ of the output waveform.

rest time

19. Refer to figure 4.

The two functions of C11, R20, R17 are to

a. determine the rest time of the output waveform.

b. form a variable discharge path for C11.

c. provide control of the output trigger voltage.

d. provide the triggering voltage for Q3.

P.I.	Module 5-5 Lesson Topic 5-5-1
a, d.	20. Refer to figure 4. C11 discharges from T0 to ________ through L1 and R22. The combination L1 and R22 determines the duration of the output pulse and ________ the output waveform.
T2 develops	21. Which of the following statements correctly describes the function of Q3 in the unijunction trigger oscillator? a. Q3 is a switch to provide a discharge path for C11 from T0 to T2. b. Q3 is a switch to complete the charge path for C11 from T2 to T3. c. Q3 provides flywheel path for the tank circuit from T0 to T1. d. Q3 amplifies the output waveform.
a.	22. The RC time of C11, ______, and ______ determines the charge time of C11. When C11 charges to approximately 8 volts, ______ is triggered into conduction. (Figure 4)

P.I.	
R17 R20 Q3	23. In the figure below, two circuit functions of the series combination L1 and R22 are to a. develop reverse bias for Q3 from T0 to T2. b. determine the discharge time of C11. c. provide regenerative feedback to sustain oscillations. d. develop the output waveform.

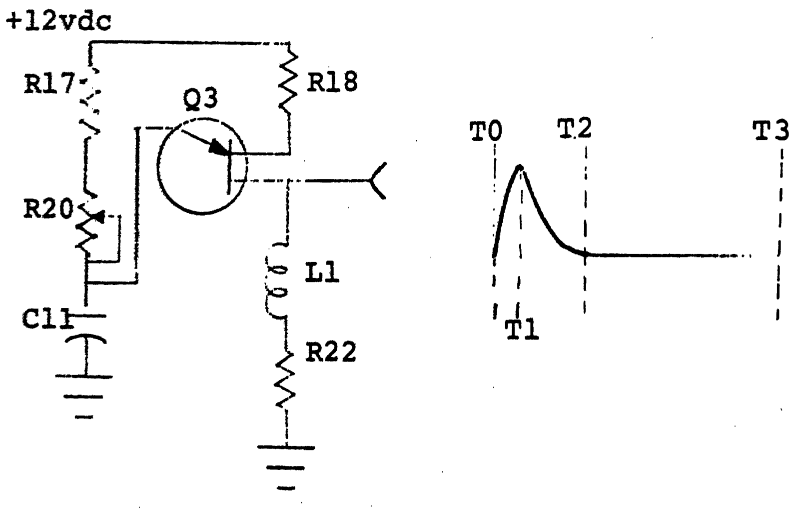


FIGURE 6

P.I.	
b, d.	24. Referring to figure 6, two functions of the series combination R17, R20, and C11 are to a. determine the rest time of the output voltage waveform. b. provide the required voltage to cause Q3 to conduct. c. provide regenerative feedback to sustain oscillations. d. compensate for the voltage drop across L1 and R22 to ensure sufficient output amplitude.
a, b.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 2

BOOTSTRAP SAWTOOTH GENERATOR

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-2

BOOTSTRAP SAWTOOTH GENERATOR

In this lesson topic the Sweep Gate Generator card (A3A2) circuit configuration and circuit operation will be covered.

The learning objectives for this lesson topic are as follows:

1. Select from a list the statements that describe the configuration and overall operation of the bootstrap sweep generator, associated gating circuits, and sweep stop comparator.

2. Select from a list statements that describe the operation of the bootstrap sweep generator on the Sweep Generator Card (A3A2) in system operation with 50 mile range selected.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-2

BOOTSTRAP SAWTOOTH GENERATOR

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

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1. Job Program in Job Program Booklet.
2. Student response sheets.
   a. Job Data sheet.
   b. Answer sheet for use with test.
   c. Programmed instruction response sheets.

ENRICHMENT MATERIALS:

1. Airborne Search Radar Training Device, 15A21 Maintenance Instruction Manual.
2. Basic Electronics, Vol. II, NAVPERS 10087-C, Ch. 4, pp. 68-74.

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

BOOTSTRAP SAWTOOTH GENERATOR

INTRODUCTION

In this lesson topic you will learn about the Sweep Gate Generator card A3A2 within the synchronizer of the Airborne Search Radar System Trainer. The first section will include the configuration and overall operation of the Sweep Gate Generator card, A3A2. This circuit card contains the following three main circuits:

a. Sweep gate generator.
b. Bootstrap sweep generator.
c. Sweep stop comparator.

The second part of the lesson topic will deal with the operation of the Bootstrap sweep generator. The complete circuit analysis is covered in stages to provide a better understanding of the circuit operation and the components affecting the output waveform. At the end of the lesson topic, a laboratory assignment will provide further study of the circuit operation.

P.I.

1. Refer to the schematic diagram of the sweep generator card (A3A2). In the lesson topics on the detailed block diagram, it was shown that this card contains two circuits; the sweep gate generator, and the bootstrap sweep generator. On the schematic the sweep gate generator circuitry includes U1 and its associated components. U1 is an integrated circuit inverter and set-reset flip-flop. U1A is wired to invert the positive-going sync trigger pulse input. The inverted pulses are applied to U1D, causing U1D-Pin 11 to go high. This initiates the positive sweep gate (T0). With pin 11 connected directly to U1C-pin 10, the change in pin 11 is felt on pin 10 (Pin 9 connected to U2 is normally high), causing the output of U1C (pin 8) to change to the low-state (T0).

1. (Continued)

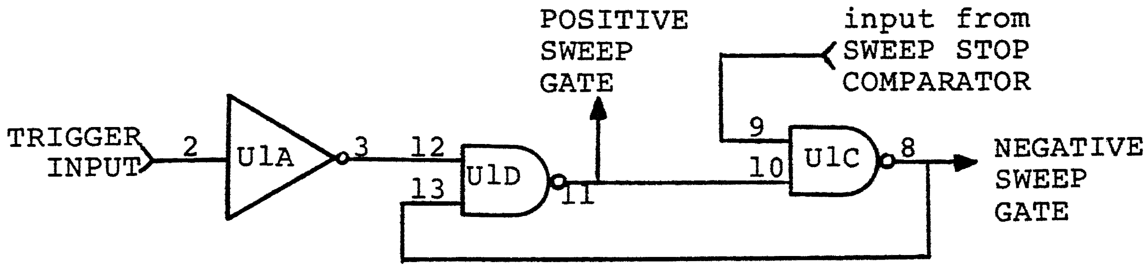


FIGURE 1 - SWEEP GATE GENERATOR (U1)

The circuit will remain in this state until the sweep is terminated by U2. U2 is another integrated circuit package used as a voltage level comparator circuit. U2 compares the amplitude of the sweep sawtooth to a fixed reference voltage. When the sweep sawtooth voltage exceeds the preset reference, the output of U2 changes from high to low and this change is applied to U1C Pin 9. This switching action will reset the flip-flops U1C and U1D (T1) terminating the sweep gate until the next sync trigger is applied. The output of U2 is at pin 7 and is called the <u>sweep stop pulse</u>.

P.I.	
	1. (Continued) The two input signals to the sweep gate generator are the ________________ __________, and, from U2, the __________ _____________ _______________.
sync trigger sweep stop pulse	2. The sweep gate generator provides two output squarewaves of voltage. The positive and negative sweep gates are applied to the range marks card (A3A3) and the Radar Display Indicator (A4). The negative gate is also applied to the bootstrap sweep circuit to initiate the sweep. The outputs of the sweep gate generator U1 are the _________ and ____________ sweep gates.

P.I.	
positive negative	3. The input signals to the sweep gate generator, A3A2U1, are the ____________ ____________ and the ____________ ____________ pulse. The outputs from the sweep gate generator are the ____________ and ____________ sweep gates.
sync trigger sweep stop positive negative	4. Refer to the schematic diagram of the Sweep Generator Card. The bootstrap sweep generator is made up of transistors Q1, Q3, Q4, and CR2 along with the RANGE switch and controls on the synchronizer chassis and indicator panel. Transistor Q4 functions as a high speed switch, Q3 and Q1 are emitter-followers; Q3 develops the positive going sweep sawtooth and provides current feedback to C4, Q1 provides impedance matching and current gain for the low level sweep output.

P.I.	
	4. (Continued) Transistor Q4 functions as a ____________ ____________ __________, Q3 develops a ____________ going sweep sawtooth, and the function of Q1 is impedance matching and current gain for the ____________ ____________ sweep output.
high speed switch positive low level	5. Match the transistors with their circuit function. a. Q4. b. Q3. c. Q1. (1) Develops the positive sweep voltage and provides current feed-back to C4. (2) High speed switch. (3) Final output amplifier for the sweep gate. (4) Impedance matching and current gain for the Low Level sweep. (5) Establishes the reference voltage for sweep stop comparator.

P.I.	
a2, b1, c4.	6. The input signals to the sweep Gate generator are the sync ___________ and the sweep __________pulse. Each of these inputs changes the conducting state of U1 thereby generating the ________ and negative sweep ________________.
trigger stop positive gates	7. Refer to the schematic diagram of the Sweep Generator Card, A3A2. The output from the bootstrap sweep generator is applied to three points within the synchronizer. These points are: a. Sweep stop comparator (U2). b. Resolver driver card (A3A1). c. To test point (I) on the A3A2 card. The sweep sawtooth applied to the sweep stop comparator U2, is compared to a fixed reference voltage to establish the required sweep amplitude and gate duration. The output applied to the resolver driver card (A3A1) is the Low Level Sweep. The secondary test point (I) is on terminal board A3A2TB1, and is used to monitor the bootstrap sweep generator output.

P.I.	
	7. (Continued) The low level output from the emitter follower Q1 is applied to the ____________ ________________ ________________ and to the _____________ _______________ card.
sweep stop comparator resolver driver	8. The bootstrap generator output is applied to the sweep stop comparator, sweep resolver and a test point. TRUE/FALSE.
FALSE	9. In the bootstrap circuit, transistor ____________ acts as a high speed switch, Q ________ develops a positive going sweep and provides current feedback to C4, and _________ provides impedance matching and current gain for the low level sweep.

P.I.	
Q4, Q3, Q1.	10. The ____________ ____________ and the ____________ ____________ pulse are inputs to the sweep gate generator and the ____________ and ____________ sweep gates are the outputs.
sync trigger sweep stop positive negative	11. Refer to the schematic of the Sweep Generator Card A3A2. The input to the sweep stop comparator (U2) is the low level sweep voltage. U2 compares this voltage to a fixed dc reference voltage. When the low level sweep voltage exceeds the fixed reference voltage, the output of the comparator (pin 7) switches low for a period long enough to reset the flip-flop (U1C). This ends the sweep gates, thus ending the bootstrap generator output. The input signals to the sweep stop comparator are the ____________ ____________ sweep and a ____________ dc reference voltage.

P.I.	
low level fixed	12. The low level sweep and a fixed dc reference voltage are the inputs to the __________ __________ __________, U2.
sweep stop comparator	13. The output of the bootstrap generator is applied to the sweep ________ comparator, and to the sweep resolver driver card as the ________ __________ sweep.
stop low level	14. Match the circuit functions to the components on the Sweep Generator Card, A3A2. a. Q4. b. Q3. c. Q1. (1) Establishes the reference voltage for the sweep stop comparator, U2. (2) Functions as an emitter follower to provide impedance matching and current gain for the output low level sweep. (3) Emitter follower and develops positive-going sweep sawtooth. (4) Switch to turn the sweep circuit on or off. (5) Final output amplifier for sweep gate.

P.I.	
a4, b3, c2.	15. The Sweep Stop Comparator input signals are the low level ______________ and a fixed ___________ ____________ voltage.
sweep dc reference	16. Refer to the schematic of the Sweep Generator Card, A3A2. Where is the output of the bootstrap sweep generator applied? (Select three) a. Sweep gate generator. b. Sweep stop comparator. c. Sweep resolver driver card. d. To a test point on the A3A2 card.
b, c, d.	17. Select two input signals to the sweep stop comparator (U2). a. Dc reference voltage. b. Sweep control voltage. c. Positive sweep gate. d. Low level sweep. e. Negative sweep gate.

P.I.	
	18. In low amplitude sweeps, the sawtooth waveform may be adequate for the desired linearity, but for higher amplitude sweep voltages, the linearity of the transistor sweep generator output is inadequate. To overcome this problem another type of sawtooth waveform generator was developed; the bootstrap sweep generator. The bootstrap sweep generator develops a linear sawtooth of voltage which has a relatively large amplitude. The bootstrap sweep generator develops this higher amplitude waveform by maintaining a nearly constant charging current to the sweep capacitor in the circuit. A bootstrap sweep generator produces a linear ________________ waveform with high amplitude.
sawtooth	19. To develop a linear sawtooth of voltage with a relatively large amplitude, radar systems use a. sawtooth generators. b. miller sweep generators. c. bootstrap sweep generators.

P.I.	
c.	20. Refer to the schematic of the Sweep Generator Card A3A2 (Refer to Figure 2-26 of the MIM). The sweep is started by the leading edge of the negative sweep gate applied to Q4 from U1C, pin 8, cutting Q4 off. C4 will start to charge. C4's charging circuit is through a resistor-potentiometer combination, the RANGE switch and diode CR2 to the +12 vdc source. The resistor-potentiometer combination connected to C4 is selected by the RANGE switch on the indicator panel. As the range selection is increased, the RC time of the charge path of C4 is proportionally increased to produce sweep waveforms with longer rise times. Potentiometer R24 and resistor R25 form the 50-mile range timing resistance connected in series with C4 to form the linear sweep sawtooth waveforms. In the 25-mile range, potentiometer R19 and resistor R20 are connected to C4. In the 2-20 mile range, resistor R18 is connected in series with the 2-20 mile range control on the indicator.

P.I.	
	20. (Continued) NOTE: In independent operation, resistor R17 and potentiometer R15 perform the function of the indicator RANGE control for the 2-20 mile range. Refer to the schematic of the Sweep Generator Card, A3A2. With the 50-mile range selected the charge path for C4 is through __________, __________, __________, __________, __________.
R25, R24, Range Switch, CR2.	21. When the range switch is positioned to the 25-mile range, C4 is connected in series with which components to form the range timing network? (Figure 5-8). (Select two) a. R19. b. C5. c. R18. d. R20. e. R15.
a, d.	22. The high amplitude linear sweep voltage is the function of the __________ __________ generator.

P.I.	Module 5-5 Lesson Topic 5-5-2
bootstrap sweep.	23. When the negative sweep gate switches Q4 off, C4 charges towards +12 vdc through the selected range timing resistance and diode CR2. The emitter follower Q3 will apply this change (C4 charging) to Ql and through C5 to the cathode of CR2. The feedback from Q3 through C5 is the sweep control voltage. As the base voltage at Q3 rises in the positive direction with the charging of C4, this voltage is added to C5's charge, cutting off CR2, and is applied to one end of the selected timing resistance. Hence, C4, at the start of the start of the sweep, initially charges toward +12 volts through CR2. As the output of Q3 increases, and the feedback through C5 is added to the charge on C5, C4 charges towards this new value of voltage. The result is <u>a near constant charging current</u> through C4. A constant current in C4 causes a linear voltage rise instead of the exponential rise that could be expected without feedback through C5.

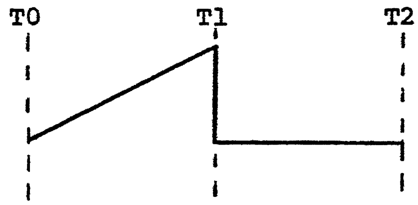
P.I.	
	23. (Continued) C5 in the bootstrap sweep generator provides a feedback of __________ __________.
constant current	24. The function of C5 in the bootstrap sweep generator is to a. provide a reference voltage for the sweep amplitude. b. provide a constant current source for the charge of C4. c. provide a complete charge path for C4.
b.	25. Refer to the schematic of the Sweep Generator Card A3A2. After the leading edge of the negative sweep gate cuts off Q4, the charge path for C4 with 50 mile range selected is a. R21, Q3, C4. b. R21, R1, and Q1 in parallel with R9, Q3, C4. c. R21, C4, R25, R24, Range switch and CR2.

P.I.	
c.	26. The function of the bootstrap sweep generator is to a. determine the electrical length of the sweep. b. generate a high amplitude pulse to trigger the sweep. c. develop a high amplitude linear sawtooth voltage. d. generate a high amplitude square pulse for sweep triggering.
c.	27. Capacitor C5 charges to the applied voltage and with the extremely long time constant will provide feedback when CR2 is cutoff. As the emitter voltage of Q3 increases, C5 will couple this charge to the cathode of CR2. When CR2 cuts off the capacitor C5 provides the constant current to C4. The charge path for C5 is -12 vdc, R9 in parallel with R1 and Q1, C5, CR2, to +12vdc. List the components in the charge path of capacitor C5. ______________________ ______________________________.

P.I.	
-12 vdc, R9 in parallel with R1 and Q1, C5, CR2, to +12vdc.	28. The charge path for C5 is the a. parallel path of R9, Q1, R1, and CR2. b. parallel path of R21, C4, Q1, and CR2. c. parallel path of R9, Q3, R1, and CR2.
a.	29. The constant current source in the bootstrap sweep generator is provided by __________ which charges through -12 vdc, __________ in parallel with R1 and __________, C5, and __________, to +12 vdc.
C5, R9, Q1, CR2.	30. Refer to the schematic of the Sweep Generator Card (A3A2). With the 50-mile range selected, the charge path of C4 is a. C4, R25, R24, range switch, CR2. b. Q4, C4. c. A3, C4. d. R9, Q3, C4, e. C4, R25, R26, Q1, CR2.

P.I.	
a.	31. Referring to the schematic of the Sweep Generator Card, the size of C4 is .033uf and the size of C5 is luf. The relationship of the size of C5 to C4 is that C5 is many times the size of C4. As in the Simplified Counters lesson topic (5-4-5) the size of the capacitor has a direct relationship on the amount of charge on the capacitor. Since C5 is many times the size of C4, a small change in the charge on C5 will result in a large change in the charge on C4. What is the relationship between C5 and C4 in the bootstrap sweep generator?__________ ____.
C5 is many times the size of C4.	32. The size relationship of C5 to C4 is that a. C4 and C5 are equal. b. C4 is many times larger than C5. c. C5 is many times smaller than C4. d. C5 is many times larger than C4.

P.I.	
d.	33. The purpose of the feedback circuit (C5) in the bootstrap sweep generator is to a. provide a complete charge path for C4. b. provide a complete discharge path for C4 c. provide a constant current source for the charge of C4. d. provide a reference voltage for the maximum sweep amplitude.
c.	34. When C4 starts to charge, the positive change in voltage appears at the emitter of Q3 and is added to the charge on C5, diode CR2 will cut off. This disconnects the +12vdc applied voltage and the source of charging current is now C5. C5, by discharging slightly, maintains a constant voltage across the resistor potentiometer network. The diode CR2 is ____ ____ during the charging of capacitor C4.

P.I.	
cut off	35. During what circuit action and time period is CR2 cut off?  FIGURE 2: LOW LEVEL SWEEP a. While C4 is discharging. b. While C5 is discharging. c. From T0-T1. d. From T1-T2.
b, c.	36. Refer to the schematic diagram of the Sweep Generator Card, A3A2. The relationship of the value of C5 to C4 is that C5 is many times ______ (smaller/larger) than C4.

P.I.	
larger	37. When the negative sweep gate trailing edge causes Q4 to go into conduction, the capacitor C4 is provided with a discharge path. When Q4 conducts the discharge path for C4 is C4, to ground, Q4 emitter collector, C4. This path for discharge of C4 is very short. This short discharge time gives the output sawtooth of voltage a very sharp trailing edge. The discharge path for C4 is ground, transistor _________, C4.
Q4.	38. The components in the discharge path of C4 are: a. C4, Q3. b. C4, Q3, C5, CR2. c. Q4, C4.
c.	39. Refer to Figure 4. During the time period of T0-T1 the diode CR2 is ____________ _________ and C5 is discharging.

P.I.	
cut off	40. Refer to the schematic diagram of the Sweep Generator Card. The statement that correctly describes the relationship of the value of C5 to C4 is that a. C5 is many times smaller than C4. b. C5 is twice the value as C4. c. C5 is half the value of C4. d. C5 is many times larger than C4.
d.	41. The bootstrap sweep generator output is applied through Q1 to the sweep stop comparator and to test point TB1-2. This waveform (Low Level Sweep) is shown below in synchrogram with the Negative Sweep Gate waveform at TB1-5.

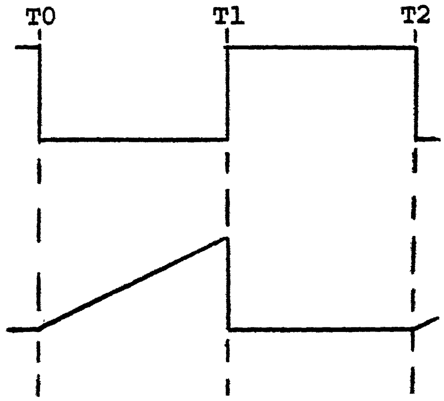


FIGURE 3

P.I.

41. (continued)

The sweep voltage is developed from T0 to T1. During this period the transistor Q4 is held cutoff by the negative sweep gate and C4 charges. Q4 conducts from T1 to T2 because it is forward biased by the positive pulse width of the negative sweep gate. The time from the end of one sweep (T1) to the beginning of the next sweep (T2) is used to discharge C4 and allow the sweep trace to return to the center of the display-indicator.

Refer to figure 3. Q4 is ____________ from T0 to T1 and ____________ from T1 to T2.

P.I.	Module 5-5 Lesson Topic 5-5-2
cut off conducting	42. What are the conduction levels of Q4 during one cycle of the below waveform?

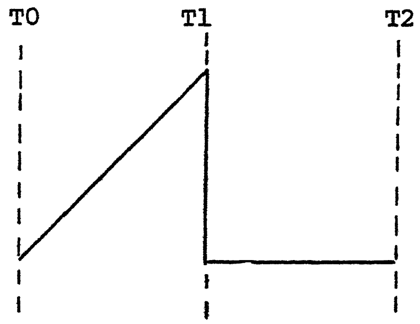


FIGURE 4

a. T0-T1 cutoff, T1-T2 cutoff.

b. T1-T2 conducting, T0-T1 conducting.

c. To-T1 cutoff, T1-T2 conducting.

c.	43. Q4 is part of the ___C4/C5___ ___charge/discharge___ path at the end of sweep time (T1).

P.I.	
C4, discharge	44. During what circuit action and time period does CR2 cutoff? a. While C4 is discharging. b. While Q4 is conducting. c. While C5 is discharging. d. From T0 to T1. e. From T1 to T2.
c, d.	45. From T0 to T1 the sweep capacitor C4 charges through the resistor-potentiometer combination selected by the Range Switch. When Q4 conducts at T1 the capacitor, C4, will discharge due to this conduction and C5 will charge to near the applied voltage.

45. (Continued)

During which portion of the waveform below does capacitor C4

a. charge________________.

b. discharge ____________.

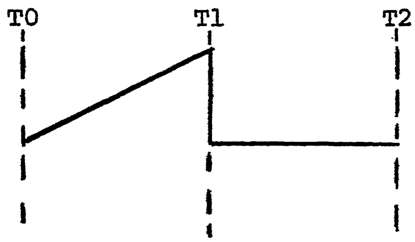


FIGURE 5

a. T0-T1.

b. T1-T2.

46. During what time period does C4 charge?

a. From sweep start to the end of sweep.

b. Only when Q4 conducts.

c. From end of sweep to start of sweep.

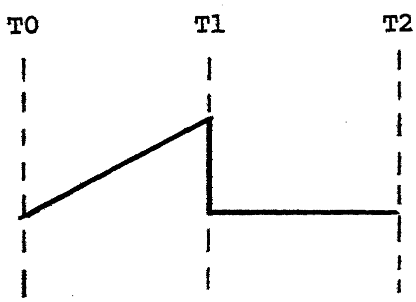
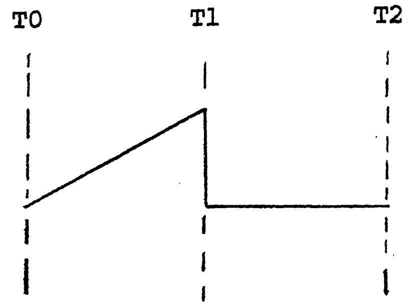


FIGURE 6

P.I.	
a.	47. In the waveform below, Q4 is ________ from T1-T2 and ______ ______ from T0-T1.  FIGURE 7
conducting cut off	48. Refer to the schematic diagram of the Sweep Generator Card, A3A2. The components in the discharge path of C4 are a. Range Switch, R24, R25, C4. b. R1, and Q1 is parallel with R9, Q3, C4. c. CR2, C5, Q3, C4. d. Q4, C4. e. R9, Q3, C4.

P.I.	
d.	49. Refer to figure 8. From T0 to T1 of the output C4 is __________ and at T1 C4 is ______________.
charging discharging	50. From the start of one sweep to the start of the next sweep, the conduction levels of Q4 are:

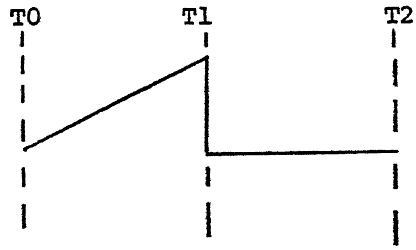


FIGURE 8

50. From the start of one sweep to the start of the next sweep, the conduction levels of Q4 are:

a. Conducting from sweep start to the end of sweep time and cutoff from end of sweep to sweep start.

b. Conducting throughout entire cycle.

c. Cutoff from sweep start to end of sweep time, conducting from end of sweep till C4 discharges, then cutoff until sweep starts.

d. Cutoff from sweep start to end of sweep time, conducting from end of sweep to sweep start.

P.I.	
d.	51. During what time period does C4 charge? a. Only when Q4 is conducting. b. From the end of sweep time to sweep start. c. From the sweep start to end of sweep. d. Only when CR2 is conducting.
c.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 3

DIFFERENTIAL LEVEL COMPARATOR AND BIAS NETWORK

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-3

DIFFERENTIAL LEVEL COMPARATOR AND BIAS NETWORK

In this lesson topic the sweep stop comparator circuit on the sweep generator card will be discussed. This lesson topic will cover the schematic circuit configuration and the funciton of the components in the circuit.

The learning objectives for this lesson topic are as follows:

1. Select, from a list, the logic symbol that represents the integrated circuit of the differential level comparator.

2. Select, from a list, the components on the sweep generator card that make up the input circuits to the differential level comparator.

3. Select, from a list, the statement that describes the function of R14 in the differential level comparator on the sweep generator card.

4. Select, from a list, the statement that describes the function of U2 in the differential level comparator on the sweep generator card.

5. Select, from a list, the circuit symbols for the components that perform the functions of decoupling and isolation in the differential level comparator.

*6. Given an airborne search radar system trainer, its MIM, and appropriate test equipment, measure and record voltages and waveforms at designated test points.

NOTE: All objectives for this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

* Accomplished in lab.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-3

DIFFERENTIAL LEVEL COMPARATOR AND BIAS NETWORK

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following study resources.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS:

1. Job Program in job program booklet.
2. Student response sheets
   a. Job Data sheet.
   b. Answer sheet for use with test.
   c. Programmed instruction response sheets.

ENRICHMENT MATERIAL:

Maintenance Instruction Manual (MIM) 15A21.

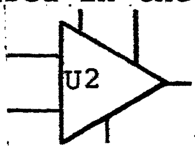
All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

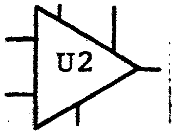
PROGRAMMED INSTRUCTION

DIFFERENTIAL LEVEL COMPARATOR AND BIAS NETWORK

INTRODUCTION

In this lesson topic the Sweep Stop Comparator circuit operation and configuration will be discussed. The preceding lesson topic explained that the sweep stop comparator output is applied to the sweep gate set-reset flip-flop to "reset" the sweep gates which are used to stop the bootstrap sweep generator's sweep voltage. Refer to figure 5-8 in the MIM during the circuit descriptions.

1. On the sweep generator card schematic, the logic symbol used in the differential level comparator is, 

and is located in the upper right-hand corner. This symbol denotes the connection of external components and power connections to specific pin locations. When the differential level comparator is used on the sweep generator card, it is called a sweep stop comparator. The logic symbol used in the differential level comparator is 

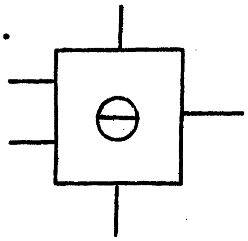
TRUE/FALSE

P.I.

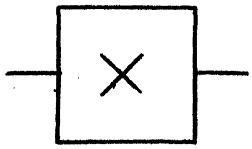
True

2. Select the logic symbol used in the differential level comparator.

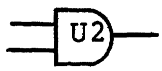
a.



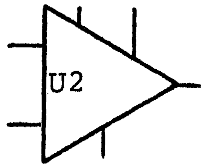
b.



c.



d.



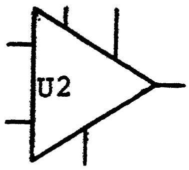
d.

3. Refer to the sweep generator card schematic diagram in the MIM. The logic element labeled U2 is a high-gain integrated-circuit differential amplifier. U2 has two inputs; a non-inverting input (Pin 2), and an inverting input (Pin 3). The difference between the two inputs is that the inverting input changes the polarity (or logic) of the signal applied and the non-inverting does not. Resistors R6 and R10, connected to Pin 3 of U2, develop the sawtooth input applied to Pin 3. Potentiometer R14 establishes a threshold (reference) voltage between 0 vdc and +12 vdc on Pin 2 of U2.

P.I.	Module 5-5 Lesson Topic 5-5-3
	3. (Continued) The three components, R6, R10, and R14 form the input circuit to U2, and these components in conjunction with U2 form a differential level comparator (sweep stop comparator). The components that comprise the input circuitry for the differential level comparator are ____________, ____________, and potentiometer ________________.
R6, R10, R14	4. Refer to the schematic diagram of the sweep generator card. The input circuit components of the sweep stop comparator are: a. C15, R1. b. Q1, C1, R11. c. R10, R14, R11. d. R6, R10, R14. e. R6, R10.

d.

5. Draw the logic symbol that is used in the sweep stop comparator circuit.



6. The potential (0 to +12 vdc) applied to non-inverting input, pin 2, of sweep stop comparator U2 is obtained from the wiper arm of R14. This potential on pin 2 is referred to as threshold voltage. The amplitude of the sawtooth applied to inverting input, pin 3, of the sweep stop comparator, must exceed the threshold voltage on pin 2 before the sweep stop comparator will change state.

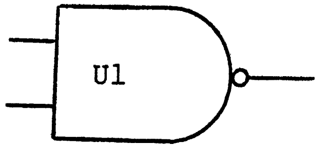
Potentiometer R14 establishes the ________ ____________ which is applied to pin______ of U2.

threshold voltage 2 (two)	7. The function of potentiometer R14 in the sweep stop comparator (U2) is to a. provide a feedback path for the bootstrap sweep generator. b. provide forward bias for the current stabilization of U2. c. establish the threshold voltage of U2.
c.	8. Refer to the schematic diagram of the sweep generator card. The input component connected to pin 2 of the sweep stop comparator is ____________________ and the components connected to pin 3 are _____________ and ____________________.

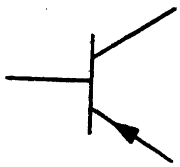
R14,
R6,
R10

9. Refer to the sweep generator card (A3A2) schematic diagram. The logic symbol used in the differential comparator is

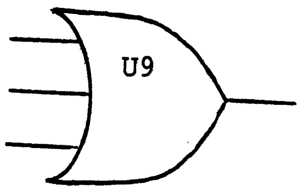
a.



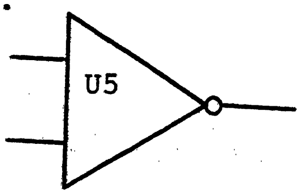
b.



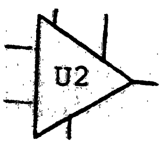
c.



d.



e.



P.I.

e. 10. The function of integrated circuit U2 is to compare the sweep signal voltage at pin 3 to the threshold voltage at pin 2 and to produce a negative (low) output pulse when the sweep voltage goes slightly higher than the threshold voltage. This pulse is observed at U2, pin 7 or TB1-4 and is a very narrow negative spike. Refer to figure 1.

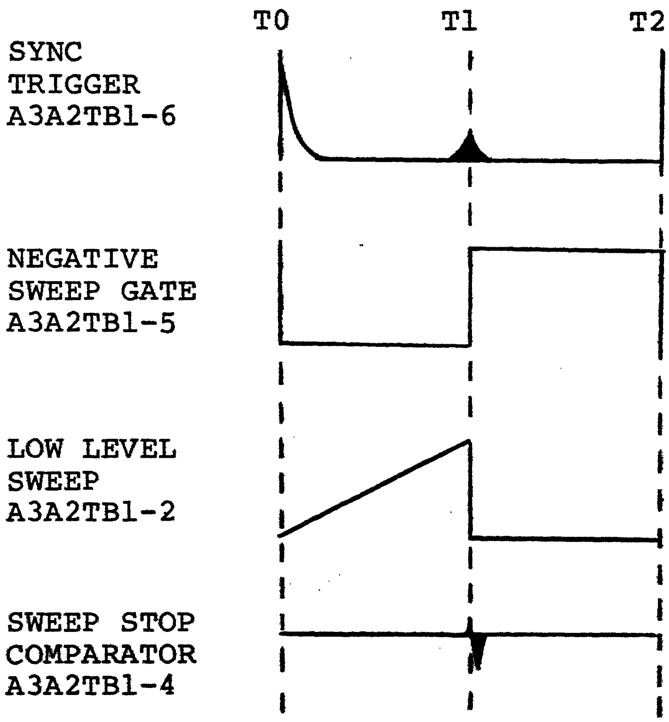


Figure 1

P.I.	
	10. (Continued) The output pulse will reset the sweep gate generator flip-flop, ending the sweep gate and stopping the development of the sweep voltage. The function of integrated circuit, U2, is to compare the ______________ voltage to the ______________ voltage.
sweep threshold	11. Comparison of the sweep voltage and the threshold voltage is the function of which component(s) in the sweep stop comparator circuit? a. U1, CR2. b. Q4, Q3, Q1. c. U2. d. Q1, R6, R10, R14.
c.	12. The component that is used to adjust the threshold voltage applied to the sweep stop comparator circuit is ________________.

P.I.	
R14	13. Refer to the sweep generator card schematic diagram. The input components of the differential level comparator are: a. C15, R1, U2. b. R6, R10, C11. c. R6, R10, R14. d. C15, R6, R10.
c.	14. Refer to figure 2 on the following page and to figure 5-8 in the MIM. Capacitor C1, identified by a shaded area on figure 2, is part of a decoupling network in the +12 vdc line coming from the ± 12 vdc synchronizer power supply. A decoupling network is a combination of capacitors, resistors, or inductors used to prevent interstage coupling of unwanted signals. In this case, it prevents the coupling of noise between all the stages connected to the +12 V line. Capacitor C1 is paralleled by two other capacitors, C13 and C14, located in the +12 V line at the bottom of figure 5-8. R11 has no effect on the operation of the sweep stop comparator. It is an isolation resistor for test point A3A2TB1-4. When an oscilloscope or test meter is connected to the test point, R11 prevents loading of the circuit under test. Isolation resistors are used throughout all types of avionics equipment.

14. (Continued)

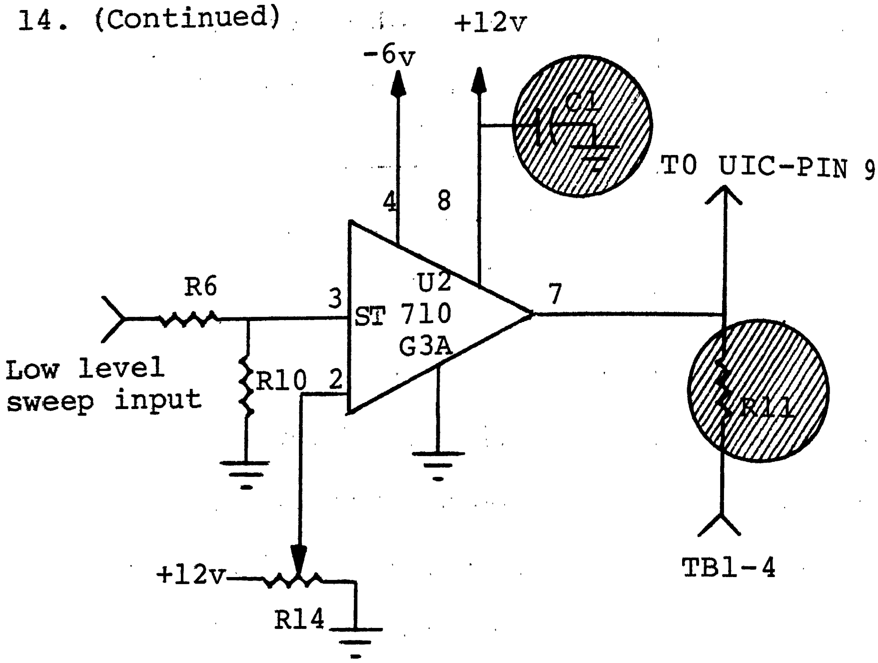


Figure 2

The components C1 and R11 provide

________________ and ________________
coupling/decoupling isolation/coupling

in the sweep stop comparator circuit.

---

decoupling

isolation

15. In the sweep stop comparator circuit, C1 provides ______________ of any noise in the dc power line and R11 provides ______________ for test point A3A2TB1-4.

P.I.	Module 5-5 Lesson Topic 5-5-3
decoupling isolation	16. The function of U2, in the differential level comparator, is to ________________ the __________________________ voltage to the ____________________________ voltage.
compare sweep threshold	17. Refer to the schematic diagram of the sweep generator card. The function of R14 in the differential level comparator circuit is to: a. establish the threshold voltage at pin 2 of U2. b. attenuate the trigger pulses at pin 2 of U2. c. provide forward bias for the current stabilization circuit of U2. d. provide current feedback for Q1.

P.I.	Module 5-5 Lesson Topic 5-5-3
a.	18. Refer to figure 3. In the sweep stop comparator, C1 performs ____________ and R11 is used for ____________.

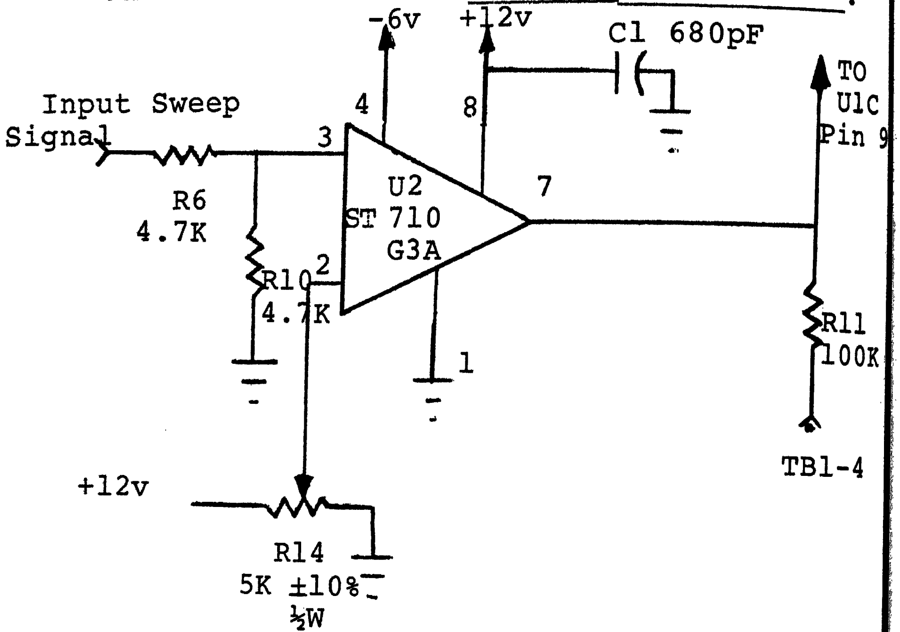


FIGURE 3

decoupling isolation	19. The function of U2 in the differential level comparator on the sweep generator card A3A2 is to a. compare the sweep voltage with the threshold voltage. b. compare the positive sweep gate with the negative sweep gate. c. initiate a digital countdown. d. establish sweep fall time.

P.I.	Module 5-5 Lesson Topic 5-5-3
a.	20. Refer to the sweep generator card schematic diagram. The two components that perform the functions of decoupling and isolation in the differential level circuit are a. R15 and R6. b. R14 and R4. c. R6 and R10. d. C1 and R11.
d.	At this point, you may take the lesson topic check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 4

GATED FIELD EFFECT TRANSISTOR (FET) AND CLAMPING NETWORK

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-4

GATED FIELD EFFECT TRANSISTOR (FET) AND CLAMPING NETWORK

In this lesson topic the construction and schematic symbol of the field effect transistor (FET) and the sweep clamping network of the sweep processor cards (A4A3) and (A4A4) will be covered. The operation of the sweep clamping network is covered by simplifying the circuit operation and completing a laboratory assignment showing the actual circuit changes in NORMAL and DEPRESSED CENTER operation.

The learning objectives for this lesson topic are as follows:

1. Select from a list, the names of the elements of a field effect transistor.

2. Refer to the schematic diagram for the sweep processor card. Select the symbol for the field effect transistor.

3. Select from a list, the function of the field effect transistor in the sweep clamping network.

4. Select from a list the purpose of the field effect transistor in the sweep clamping network.

5. Refer to the schematic diagram of the sweep processor card. Select the semiconductor devices used in the sweep clamping network.

6. Refer to the schematic diagram of the sweep processor card. Select the electromechanical device used in the sweep clamping network.

7. Select from a list the voltage that establishes the conduction state for Q9 in the sweep clamping network.

8. Select from a list the voltage that controls the conduction of Q8 in the sweep clamping network.

9. Select from a list the voltages that establish the reference for C2 in the sweep clamping network.

10. Select from a list the voltages that affect the sweep clamping functions.

11. Select from a list the effects of the relay operation on the sweep clamping functions.

12. Select from a list the effects of the input gating waveform on the sweep clamping functions.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-4

GATED FIELD EFFECT TRANSISTOR (FET) AND CLAMPING NETWORK

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following study resources.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job program in Job Program Booklet

2. Student response sheets
    a. Job data sheet
    b. Answer sheet for use with test
    c. Programmed instruction response sheets

ENRICHMENT MATERIAL:

Maintenance Instruction Manual (MIM) 15A21

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

GATED FIELD EFFECT TRANSISTOR (FET) AND CLAMPING NETWORK

INTRODUCTION

In this lesson topic the construction and schematic symbol of the field effect transistor (FET) will be covered. The purpose and function of the FET will also be discussed.

A detailed analysis will be made of the sweep clamping network within the sweep processor card of the radar trainer display-indicator. This analysis will include the static voltage, configuration, relay operation, and input waveform effects.

We will cover the field effect transistor first.

1. The field effect transistor is a special type of semiconductor device, sometimes called a unipolar transistor and is completely different from a conventional transistor. It is made of a solid block of semiconductor material which forms the <u>body region</u> of the device. The body region contains one or two PN junctions formed by the addition of a <u>gate element</u>. The gate forms a band around the mid-section of the body region, thus producing a single PN junction

P.I.

1. (Continued)

at the point of contact.

As shown in Figure 1, the field effect transistor contains three (3) elements: the common element, called the source; the output element, called the drain; and the input (control) element, called the gate.

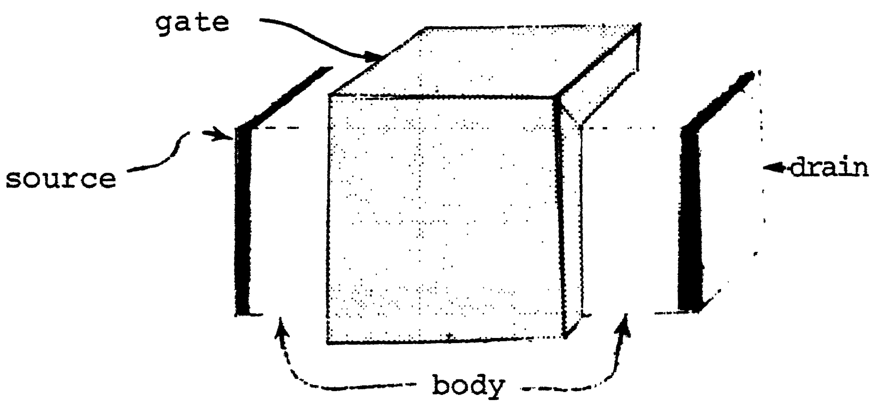
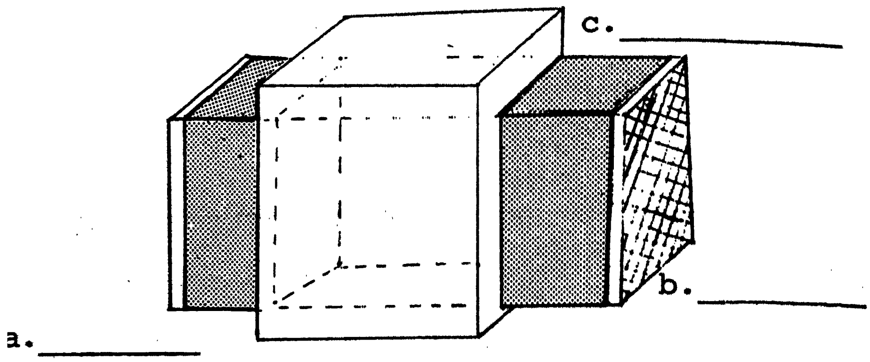


FIGURE 1

In the field effect transistor the three elements are: the common element, the ____________; the output element, the ____________; and the input (control) element is the __________.

source
drain
gate

2. Label correctly the three (3) elements of a field-effect transistor.



a. source
b. drain
c. gate

3. The schematic symbols of the field effect transistor are shown in Figure 2. Figure 2 (A) shows a P-type body and (B) shows an N-type body region.

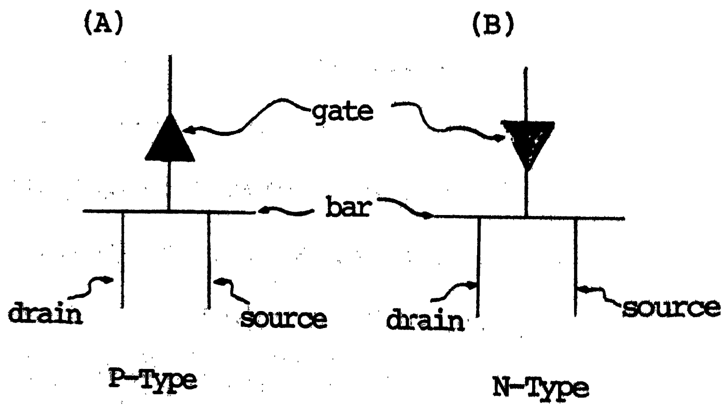
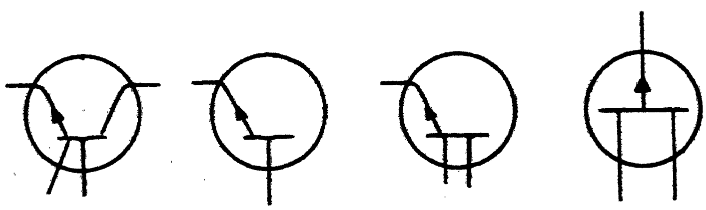


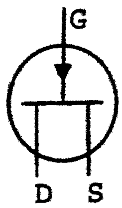
FIGURE 2

Schematic symbols of field-effect transistors - (A) P-type and (B) N-type

P.I.	
	3. (Continued) FET's are easily identified by the parallel legs on one side of the bar. The left-hand leg, with the symbol in the vertical position, represents the <u>drain</u>; the right-hand leg is the <u>source</u>; and the single leg with the arrow represents the <u>gate</u>. The direction of the arrow indicates whether the body is N-type or P-type just as the arrow in transistors indicates the type material used. Refer to the schematic diagram of the sweep processor card. The field-effect transistor is listed as Q8 and has ____________ (N-type/P-type) body material.
P-type	4. Select the schematic symbol of the field-effect transistor from the group of schematic symbols below.  A B C D

P.I.	
d.	5. The three elements of the field-effect transistor are the source, the ____________, and the ____________.
drain gate	6. The gate is the control element of the field-effect transistor. Applying a voltage to the gate produces an electrostatic field, or channel in the body region through which the current carriers flow. When the intensity of the field is increased, channel size decreases or as the field is decreased, the channel size increases. Thus, by controlling the intensity of the field, the flow of current in the body region can be controlled. The effect of a variation in barrier opposition on this current is instantaneous with respect to the gate signal amplitude. This fast circuit response allows the field effect transistor to be used as a high-frequency amplifier, as an oscillator, or as an electronic switch. On the sweep processor card schematic diagram, the field-effect transistor, Q8, performs the function of a high-speed <u>electronic</u>

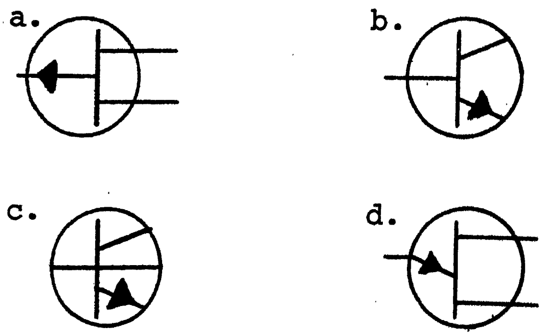
P.I.	
	6. (Continued) switch in the sweep clamping network. Transistor Q8, the field-effect transistor on the sweep processor card, functions as an ______________ ______________.
electronic switch	7. The function of Q8 in the sweep clamping network is to a. provide an oscillator circuit. b. provide high-frequency amplification. c. provide electronic switching. d. amplify the negative sweep gate.
c.	8. The source, drain, and gate are the three contacts of a FET. Draw and label the schematic symbol for an N-type field-effect transistor.

P.I.	
	9. The three elements of the field-effect transistor are: a. collector b. source c. gate d. base e. drain f. emitter
b,c,e.	10. When the NORMAL/DEPRESSED CENTER switch on the display-indicator is in NORMAL, the field-effect transistor switches a ground potential to C2 to prevent the capacitor from seeking the average dc value of the sweep waveform. In DEPRESSED CENTER operation, the transistor provides a reference voltage, from potentiometer R29, to the capacitor C2. These potentials, applied by the electronic switching of Q8, assures that the capacitor C2 assumes the proper predetermined potential at the end of sweep time.

P.I.	
	10. (continued) The purpose of Q8, during NORMAL/DEPRESSED CENTER operation, is to apply to C2 a ____________________ ____________________ at the end of sweep time.
predetermined potential	11. The establishing of a predetermined potential on C2 is the purpose of which device on the sweep processor card? a. CR5 b. Q2 c. Q8 d. CR6
c.	12. The field-effect transistor, Q8, within the sweep clamping network functions as an ____________________ ________________.

electronic switch

13. Which of the following is the symbol for a field-effect transistor?



a.

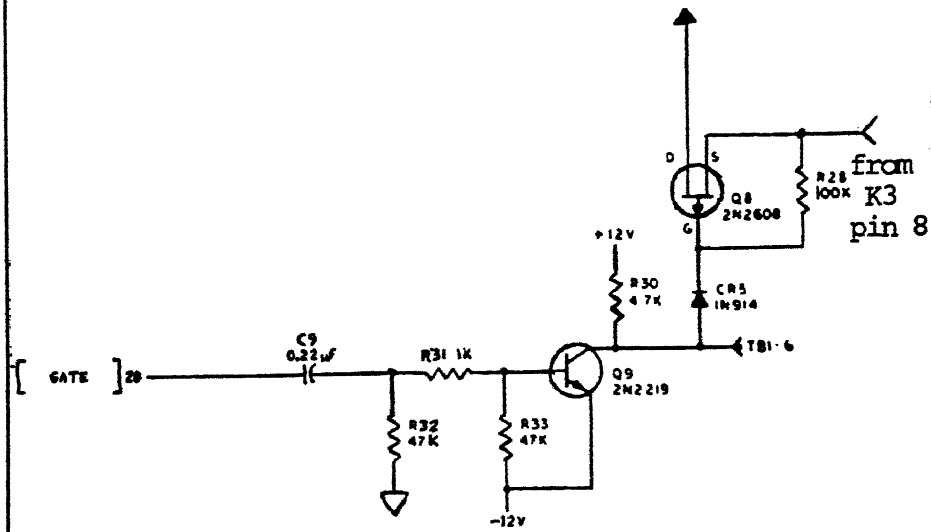
14. Refer to the schematic diagram of the Sweep Processor Card. To prevent capacitor C2 from charging to a dc value equivalent to the average value of the input, a switching circuit assures that the capacitor assumes a predetermined level at the termination of each sweep. The circuitry performing this function includes transistor Q9, diode CR5, the field-effect transistor (FET) Q8, and their associated components.

P.I.	
	14. (continued) The solid state devices used in the sweep clamping network to place C2 at the predetermined potential are: a. K3, K4, Q8. b. Q8, Q9, CR5. c. Q2, Q8, Q9.
b.	15. The solid state devices that prevent C2 from assuming the input average dc value are (select three) a. Q2 b. Q9 c. Q3 d. Q8 e. CR3 f. CR5
b,d,f.	16. During NORMAL or DEPRESSED CENTER operation, the purpose of Q8 is to provide a ____________________ potential to C2 at the end of each sweep.

P.I.	
predetermined	17. What is the function of the field-effect transistor in the sweep clamping network? a. Amplifier b. Electronic switch c. Limiter d. Gate eliminator e. Servo controller
b.	18. Refer to the sweep processor card schematic diagram. The source of Q8 is connected to pin 8, one section of relay K3. The relay K3, an electromechanical device, is connected to the NORMAL/DEPRESSED CENTER switch. When NORMAL sweep is selected, a ground is available at the source terminal, via the contacts of the de-energized relay, K3, allowing C2 to assume a zero voltage reference. When DEPRESSED CENTER (offset) is selected, relay K3 is energized and a positive voltage from R29 is applied to the Q8

P.I.	Module 5-5 Lesson Topic 5-5-4
	18. (continued) source terminal. Capacitor C2 will now maintain a charge as established by potentiometer R29. The relay ________ provides switching action for the correct sweep voltage reference.
K3	19. The relay K3 in the sweep clamping network a. provides a negative level to Q8. b. provides predetermined positive and negative voltages to Q8. c. provides switching action for the correct voltage level during NORMAL or DEPRESSED CENTER operation to Q8. d. establishes the source-to-drain potential of Q8 during sweep time.
c.	20. The solid state devices Q8, Q9, and CR5 are the ____________ circuitry that delay/switching prevents C2 from assuming the average dc value of the input signal.

P.I.	
switching	21. What is the purpose of the field-effect transistor in the sweep clamping network? a. Applies a positive voltage to C2 during normal operation. b. Amplifies the sawtooth waveform applied to Q3 during DEPRESSED CENTER operation. c. Amplifies the negative sweep gate. d. Establishes a predetermined reference for C2 at the end of each sweep during NORMAL and DEPRESSED CENTER operation.
d.	22. After the power is applied to the radar system, the bias for transistor Q9 is provided by the voltage divider consisting of R31, R32, and R33. Approximately -6vdc from the junction of R31 and R33, is applied to the base of Q9. Figure 3 shows that this base voltage and the -12vdc applied to the emitter will forward bias transistor Q9 into conduction.

P.I.	
	22. (continued)  FIGURE 3 R31, R32 and R33 establish the ___cutoff/___ ___conduction___ state of Q9.
conduction	23. The circuit voltage that establishes the conduction state of Q9 is the a. source voltage of Q8. b. emitter voltage of Q3. c. base voltage of Q9. d. gate voltage of Q8.

P.I.	
c.	24. When NORMAL or DEPRESSED CENTER is selected the device within the sweep clamping network that provides the switching action for the correct potential to Q8 is ______ ______________.
relay K3	25. Select the semiconductor devices that are used in the sweep clamping network. a. Q2, Q9, Q3. b. Q9, Q8, CR5. c. Q9, CR3, CR5. d. Q8, CR3, CR5.
b.	26. As a result of transistor Q9 being forward biased into conduction, the collector voltage of Q9 will decrease to a negative dc voltage. This negative voltage will reverse bias diode CR5. When diode CR5 is reverse biased, the gate terminal of Q8 is allowed to assume the same voltage as the source, through R28, which controls its conduction. The collector voltage of Q9 controls the conduction of __________.

P.I.	Module 5-5 Lesson Topic 5-5-4
Q8	27. The conduction state of Q8 is controlled by the a. conduction of Q9 and CR5. b. collector of Q9 and CR5 being cutoff. c. relay K3. d. the voltage on C5.
b.	28. The voltage divider R31, R32 and R33 provides the bias voltage to the base of Q9 causing Q9 to ________________. conduct/cutoff
conduct	29. Select the electromechanical device that is used in the sweep clamping network for switching action. a. K1 b. K2 c. K3 d. CR1 e. TB1-6

P.I.	
c.	30. When diode CR5 is reverse biased, the gate terminal of Q8 is allowed to assume the same voltage as the source, turning the field effect transistor Q8 on. The drain terminal is shorted to the source terminal. This will establish the reference voltage for C2. The reference voltage for C2 is the same as the ______________ voltage on Q8.
source	31. The voltage that establishes the reference for C2 is the a. grid voltage on Q8. b. base voltage on Q2. c. source voltage on Q8. d. collector voltage on Q2.
c.	32. The conduction of Q9 causes CR5 to be reverse biased. With CR5 cutoff, the gate and the source of Q8 are at the same potential. Q8 conducts and C2 assumes a charge equal

P.I.	
	32. (continued) to the voltage on the drain of Q8. The ________________ of Q9 and ___________ conduction/cutoff being cutoff, controls the conduction of Q8.
conduction CR5	33. The voltage that establishes the conduction state of Q9 is the a. source voltage on Q8. b. gate voltage on Q8. c. collector voltage on Q9. d. emitter voltage on Q2. e. base voltage on Q9.
e.	34. From the preceding frames we have found that three (3) voltages have an effect on the sweep clamping network. They are the a. biasing on the base of Q9. b. collector voltage of Q9. c. source voltage of Q8. The first two (a and b) control the conduction of Q8 and the third (c) establishes

34. (continued)

the reference voltage for C2. During NORMAL operation, a ground is available at the source and during DEPRESSED-CENTER (offset) a positive voltage is present on the source terminal.

The three voltages that affect the sweep clamping network are:

a. ___________ bias on Q9.

b. ___________ voltage on Q9.

c. ___________ voltage on Q8.

---

a. base
b. collector
c. source

35. The three voltages that affect the sweep-clamping network's function are

a. base voltage on Q2.
b. base bias on Q9.
c. collector voltage on Q9.
d. source voltage on Q3.
e. source voltage on Q8.
f. emitter bias on Q2.

P.I.	Module 5-5 Lesson Topic 5-5-4
b,c,e,	36. With CR5 cutoff, the gate terminal will assume the source voltage causing Q8 to conduct. This will short the drain to source establishing the ______ charge/reference/ ______ discharge for C2.
reference	37. The voltage that controls the conduction state of Q8 is the a. base voltage on Q9. b. source voltage on Q8. c. collector voltage on Q9. d. emitter voltage on Q2. e. base voltage on Q3.
c.	38. Refer to the schematic diagram of the Sweep Processor Card. During NORMAL operation, a ground is available at the source terminal of Q8. This potential is from the de-energized relay K3. With the relay de-energized, pins 6 and 8 are connected to ground potential. This is true for both sweep processor cards (A4A3 and A4A4).

P.I.

38. (continued)

During DEPRESSED-CENTER (offset) relay K3 is energized and a positive voltage from potentiometer R29 is applied to the source terminal of Q8. The capacitor C2 maintains an average charge as set by R29 providing the correct sweep clamping. This positive voltage is only applied in the Y-sweep processor card (A4A4). The X-sweep processor card (A4A3) has a ground connected to pin W disabling the voltage that would be developed by potentiometer R29.

The two effects of relay K3, within the Y-sweep processor card (A4A4) are

a. during NORMAL sweep, K3 applies ground potential to Q8 source.

b. during NORMAL sweep, K3 provides a cutoff voltage for Q8.

c. during DEPRESSED CENTER sweep, K3 provides a cutoff voltage for Q8.

d. applies a positive voltage to Q8 source during DEPRESSED CENTER sweep.

P.I.	
a,d.	39. Refer to the schematic diagram of the Sweep Processor Card. The effects of relay K3 operation on the sweep clamping functions are to provide a ground potential to Q8 during NORMAL sweep and to provide a positive voltage to Q8 during DEPRESSED CENTER sweep in the Y-sweep processor card (A4A4). TRUE/FALSE
TRUE	40. The three voltages that affect the sweep clamping network are the base ________ on Q9, the ________________ voltage of Q9, and the ______________ voltage of Q8.
bias collector source	41. Which voltage establishes the reference for C2 in the sweep clamping network? a. Base voltage on Q9. b. Gate voltage on Q8. c. Emitter voltage on Q9. d. Source voltage on Q8.

P.I.

d.

42. Refer to the schematic diagram of the Sweep Processor Card. The input gating waveform is a negative sweep gate applied to the base of Q9 via pin 28 of the sweep processor card. The negative portion of the gate drives transistor Q9 into cutoff. Diode CR5 is forward biased by the +12vdc applied via resistor R30. With the diode CR5 forward biased, a positive voltage is applied to the gate input of Q8 turning it off. This occurs during sweep time.

During retrace time, the positive portion of the negative sweep gate allows transistor Q9 to go back into conduction because of the static bias applied. As a result, a negative voltage is provided at the collector of Q9, reverse biasing CR5. With the diode CR5 reverse biased, the gate of Q8 is allowed to assume the same voltage as the source, turning Q8 on. The drain terminal of Q8 is shorted to the source terminal. This allows either the ground or positive potential present at pin 8 of relay K3 to be felt at capacitor C2. The switching action of Q8, as the negative sweep gate

P.I.	
	42. (continued) changes, will assure that capacitor C2 will assume the correct predetermined voltage level during NORMAL and DEPRESSED CENTER sweep operation. The switching action of Q9 and Q8 is accomplished by the _______________ sweep gate input.
negative	43. Match the effect on the sweep clamping network to the correct portion of the input negative sweep gate waveform. a. negative portion b. positive portion 1. holds Q9 and Q8 cutoff 2. drives Q2 into conduction 3. allows Q9 to conduct holding Q8 cutoff. 4. allows Q9 to conduct, driving Q8 into conduction.

P.I.	Module 5-5 Lesson Topic 5-5-4
a. 1 b. 4	44. On the Y-sweep processor card, what are the effects of relay K3 upon the sweep clamping functions? (Select two) a. K3 prevents degenerative feedback to Q8 during NORMAL and DEPRESSED CENTER. b. K3 applies a positive voltage to Q8 source during DEPRESSED CENTER sweep. c. During NORMAL sweep, K3 applies ground potential to Q8 source. d. During depressed center sweep, K3 provides a cutoff voltage for Q8.
b,c.	45. Which three of the following voltages affect the sweep clamping function? a. base bias on Q9. b. collector voltage on Q9. c. source voltage on Q8. d. base bias on Q2. e. emitter bias on Q2. f. source voltage on Q3.
a,b,c.	46. The ________________ portion of the input gating waveform causes Q9 and Q8 to cutoff and the ________________ portion will allow Q9 to conduct, driving Q8 into conduction.

P.I.	
negative positive	47. What are the two effects of relay K3 operation on the sweep clamping function on the Y-sweep processor card (A4A4). a. During NORMAL sweep, K3 applies ground potential to the source terminal of Q8. b. During NORMAL sweep, K3 provides cutoff voltage for Q8. c. During DEPRESSED CENTER sweep, K3 provides cutoff voltage for Q8. d. K3 prevent degenerative feedback to Q8 during NORMAL and DEPRESSED CENTER sweep operation. e. K3 applies a positive voltage to Q8 source during DEPRESSED CENTER sweep.
a, e.	48. What are the two effects that the input gating waveform has on the sweep clamping network? a. The negative portion holds Q9 and Q8 cutoff. b. The negative portion drives Q9 and Q8 into conduction. c. The positive portion holds Q9 and Q8 cutoff. d. The positive portion drives Q2 into conduction. e. The positive portion allows Q9 to conduct which then drives Q8 into conduction.

P.I.	Module 5-5 Lesson Topic 5-5-4
a. 1 b. 4	44. On the Y-sweep processor card, what are the effects of relay K3 upon the sweep clamping functions? (Select two) a. K3 prevents degenerative feedback to Q8 during NORMAL and DEPRESSED CENTER. b. K3 applies a positive voltage to Q8 source during DEPRESSED CENTER sweep. c. During NORMAL sweep, K3 applies ground potential to Q8 source. d. During depressed center sweep, K3 provides a cutoff voltage for Q8.
b,c.	45. Which three of the following voltages affect the sweep clamping function? a. base bias on Q9. b. collector voltage on Q9. c. source voltage on Q8. d. base bias on Q2. e. emitter bias on Q2. f. source voltage on Q3.
a,b,c.	46. The ______________ portion of the input gating waveform causes Q9 and Q8 to cutoff and the ______________ portion will allow Q9 to conduct, driving Q8 into conduction.

P.I.	
negative positive	47. What are the two effects of relay K3 operation on the sweep clamping function on the Y-sweep processor card (A4A4). a. During NORMAL sweep, K3 applies ground potential to the source terminal of Q8. b. During NORMAL sweep, K3 provides cutoff voltage for Q8. c. During DEPRESSED CENTER sweep, K3 provides cutoff voltage for Q8. d. K3 prevent degenerative feedback to Q8 during NORMAL and DEPRESSED CENTER sweep operation. e. K3 applies a positive voltage to Q8 source during DEPRESSED CENTER sweep.
a, e.	48. What are the two effects that the input gating waveform has on the sweep clamping network? a. The negative portion holds Q9 and Q8 cutoff. b. The negative portion drives Q9 and Q8 into conduction. c. The positive portion holds Q9 and Q8 cutoff. d. The positive portion drives Q2 into conduction. e. The positive portion allows Q9 to conduct which then drives Q8 into conduction.

P.I.	Module 5-5 Lesson Topic 5-5-4
a, e.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 5

DISPLAY-INDICATOR DEPRESSED-CENTER (OFF-SET) NETWORK

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-5

DISPLAY-INDICATOR DEPRESSED-CENTER (OFF-SET) NETWORK

This lesson topic covers those circuits on the Sweep Processor cards that establish the quiescent current in the CRT deflection coils and determine the starting point of the indicator sweep. The deflection of the sweep trace will be covered, as will the rotation of the sweep and the schematic symbols used to depict an electromagnetic deflection system.

The learning objectives for this lesson topic are as follows:

1. Select from a list the statement that describes the purpose of NORMAL/DEPRESSED CENTER sweep scaling network.

2. Select from a list two statements that describe the effects of K3 on the resolved sweep signal input to the differential amplifiers.

3. Select from a list the statement that describes the purpose of the differential amplifier, Q5 and Q6.

4. Complete a statement that descirbes the function of the constant current bias supply. Refer to figure 5-14.

5. Select from a list, the statement that describes the function of the "X" and "Y" feedback signals.

6. Select from a list of symbols the schematic symbol used to represent the deflection coils in an electromagnetic deflection system.

7. Select from a list of symbols the schematic symbol for a CRT which uses electromagnetic deflection.

8. Select from a list the statement that describes the phase relationship of the "X" and "Y" yoke driver sweep signals.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-5

DISPLAY-INDICATOR DEPRESSED-CENTER (OFF-SET) NETWORK

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job program in Job Program Booklet.
2. Student response sheets.
    a. Job Data sheet.
    b. Answer sheet for use with test.
    c. Programmed instruction response sheets.

ENRICHMENT MATERIALS:

1. MIM, 15A21.
2. Basic Electronics, Vol II, Ch.11.

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

DISPLAY-INDICATOR DEPRESSED-CENTER (OFF-SET) NETWORK

INTRODUCTION

During this lesson topic you will study the circuit configuration and operation of the sweep scaling network. This network is used to determine where the sweep starts and stops on the CRT during NORMAL and DEPRESSED-CENTER operation.

A description of how the resolved sweep waveforms cause the sweep to rotate on the CRT is given by analyzing the phase relationships of the sweep signals.

The symbols for the deflection coils and a cathode ray tube employing electromagnetic deflection are also covered in this lesson topic.

1. The NORMAL-DEPRESSED CENTER sweep scaling network establishes the sweep drive currents which determine where the sweep starts and stops on face of the CRT. This is done by establishing the static current levels applied to the yoke drivers. During NORMAL operation the starting point of the sweep must be in the center of the CRT and during DEPRESSED CENTER operation the

P.I.

1. (Continued)

sweep must start at the bottom edge of the CRT. (Refer to figure 1). This network also establishes the end of sweep point on the CRT during Normal and Depressed-Center.

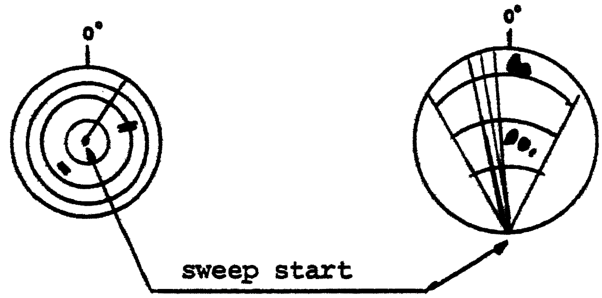


Figure 1

The purpose of the sweep scaling network is to establish the ____________ drive currents that determine where the sweep _______ and ___________ on the CRT.

P.I.	
sweep starts stops	2. The network that establishes the sweep drive currents which determine where the start and stop points of the sweep are on the CRT is the a. sweep resolver circuit. b. sweep clamping network. c. sweep scaling network. d. sweep gate generator circuit.
c.	3. Referring to figure 5-14, the relay K3 serves two functions. In lesson topic 5-5-4 it was explained that relay K3 provided the sweep clamping network with the correct reference potential for the resolved sweep during normal and depressed-center operation. (Pins 6, 7, and 8.) The second function of K3 (Pins 2, 3, and4) is to change the bias of Q5 to ensure that the sweep will start at the correct point on the CRT. This change of bias is provided by the combination of R8 in parallel with R13 and R17 when depressed center is selected. During normal operation K3 is deenergized and the resolved sweep input signal to Q5 is routed through R8.

P.I.	
	3. (Continued) The effect of relay K3 (Pins 2, 3, and 4) on the resolved sweep input, with normal selected, is that the input is routed to Q5 through ______________. In depressed center the resolved sweep is routed through the parallel combination of components ____, _______, and _________.
R8 R8, R13, R17	4. Refer to figure 5-14. Which of the components effect the resolved sweep input when K3 is a. deenergized for normal operation? (1) R4 (2) R8 (3) R7 b. energized for depressed-center operation? (Select three) (1) R4 (2) R17 (3) R18 (4) R8 (5) R13

P.I.	
a. (2) b. (2), (4), (5)	5. The ______ ______ ______ establishes the sweep drive currents which determine the sweep start and stop points on the CRT.
sweep scaling network	6. The differential amplifier (Q5 and Q6), employing a constant current source, determines the starting point of the sweep by establishing the quiescent current flow through the deflection yoke. The potentiometers in the sweep scaling network provide the correct bias, so that the correct current flows during both normal and depressed-center operations. The purpose of Q5 and Q6 is to establish the ______ current levels through the deflection yoke.

P.I.	
quiescent	7. (Refer to figure 5-14 in the MIM.) Select the two semi-conductor components that are employed to establish the quiescent current flow in the deflection yoke. a. Q1 b. Q6 c. Q7 c. VR1 e. Q5
b, e	8. In normal operation, relay K3 is deenergized routing the resolved sweep signal through component ______________ to Q5's base. With depressed-center selected, the parallel combination of _________, ___________ and ______________ route the input to Q5.

P.I.	
R8, R8, R13, R17	9. The purpose of the Normal/Depressed-Center sweep scaling network is to a. establish the amplitude of the sweep voltage. b. ensure that Q6 conducts. c. ensure that the sweep starts at the center of the scope during depressed-center operation. d. establishes the sweep drive currents which determine where the sweep starts and stops on the CRT.
d.	10. The sweep scaling provided for the differential amplifiers, Q5 and Q6, is dependent upon the function selected. The quiescent current flow through the differential amplifier is established by the constant current supplied from the bias supply circuit consisting of Q7, VR1, R23, and R25. These components make up a bias supply circuit and the output is a constant current which is applied to the emitters of the differential amplifier Q5 and Q6, (refer to figure 5-14) and provides that a constant current will flow through the <u>combination</u> Q5 and Q6.

P.I.	Module 5-5 Lesson Topic 5-5-5
	10. (Continued) The function of the constant current bias circuit is to maintain a ________ current through Q5 and Q6.
constant	11. The constant current bias supply maintains a constant current through a. Q5 only. b. Q6 only. c. Q1. d. the combination of Q5 and Q6.
d.	12. The purpose of the differential amplifier (Q5 and Q6) is to establish the ________ current flow through the deflection yoke.

quiescent	13. Refer to the schematic diagram of the sweep processor card. What are the two effects of relay K3 on the resolved sweep input to the differential amplifier? a. With normal selected, K3 is deenergized (pins 2, 4) and the input to Q5 is through R8. b. With depressed center selected, K3 is deenergized (pins 2, 4) and the input to Q5 is through R8. c. With normal selected, K3 is energized (pins 2, 3) and the input to Q5 is through the parallel combination R8, R13, and R17. d. With depressed center selected, K3 is energized (pins 2, 3) and the input to Q5 is through the parallel combination R8, R13, and R17.
a, d	14. The yoke driver feedback (pin M) is also applied to the differential amplifier. This signal is a sweep voltage proportional to the deflection coil current. The feedback signal is applied to the differential amplifier through the summing resistors R2, and R4 during NORMAL operation. During DEPRESSED-CENTER operation R8, R13, and R17 became part of the summing network.

P.I.	
	14. (Continued) This feedback is degenerative. When summed with the resolved sweep signal, the yoke driver feedback maintains the linearity of the sweep signal. The function of the yoke driver feedback signal is to provide ______________ feedback for sweep linearity.
degenerative	15. The function of the yoke driver feedback signal is to a. reduce the conduction of the sweep processor differential amplifiers. b. provide a constant conduction level in the sweep processor differential amplifier. c. provide degenerative feedback to the sweep processor differential amplifiers. d. provide a test point for the final sweep signal.
c.	16. The constant current supplied to Q5 and Q6 is the function of the ______________ ______________ bias supply circuit.

P.I.	
constant current	17. The purpose of the differential amplifier, Q5 and Q6 is to a. provide the necessary current to the yoke drivers in normal and depressed center operation. b. provide the necessary current level for the x-yoke driver in normal operation only. c. establish the quiescent current level for normal operation of the x-yoke driver. d. establish the necessary current level for the x and y yoke drivers in normal operation only.
a.	18. As you learned in the lesson topic on simplified sawtooth and trapezoidal waveform generators, there are two types of deflection systems, electrostatic and electromagnetic. The electrostatic type of deflection is commonly used in test equipment. The schematic symbol for this type of deflection is shown in Figure 2a. The symbol for electromagnetic deflection coils is shown in Figure 2b.

P.I.

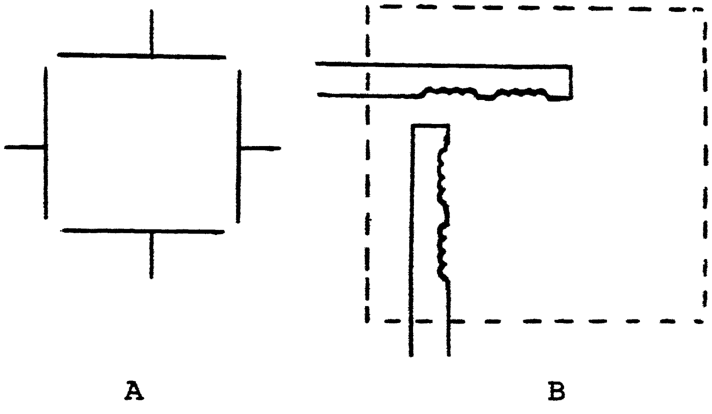
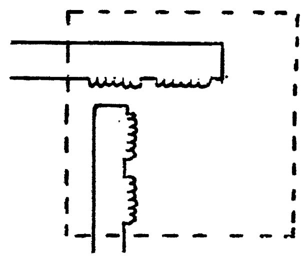


Figure 2

The electrostatic deflection system employs four (4) plates, with a sawtooth voltage waveform applied as the time base and the incoming signal applied as amplitude modulation. The electromagnetic deflection system employs the use of four (4) coils. One set of coils is for horizontal deflection and the other set is for vertical deflection. The input sawtooth current waveforms are applied simultaneously to each set of coils. Refer to figure 5-11 (sheet 2 of 2). On the right hand side are the electromagnetic deflection coils used in the display-indicator. The reference designator is A4L1.

18. (Continued)

The schematic symbol



represents an ______________________

type of deflection system.

a. electrostatic.

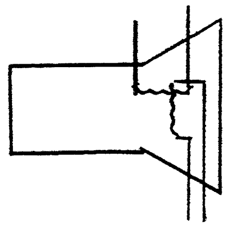
b. electromative.

c. electromagnetic.

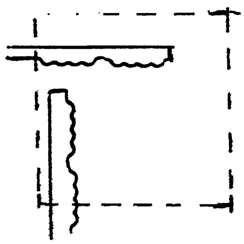
c.

19. Select the schematic symbol for deflection coils in an electromagnetic deflection system.

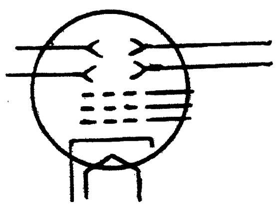
a.



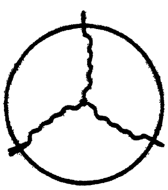
b.



c.

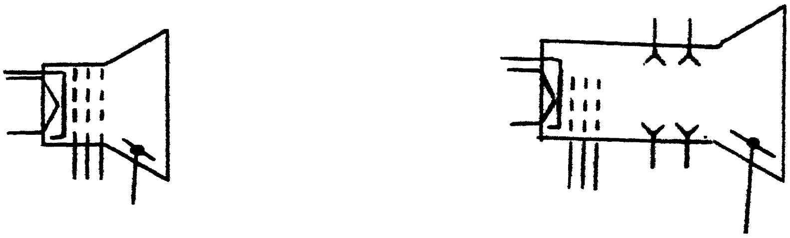


d.



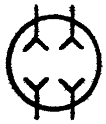
b.	20.	The degenerative feedback signal applied to the sweep processor differential amplifier is called the ____________ ____________ ____________ signal.
yoke driver feedback	21.	The function of the constant current bias supply is to maintain a constant a. current flow through Q5 b. current flow through Q6 c. bias voltage for the combination of Q5 and Q6. d. current flow through the combination of Q5 and Q6.
d.	22.	Refer to the schematic diagram of the Radar Display-Indicator Assembly. Figure 5-11 (1 of 2) On this diagram there is a pictorial view of the cathode-ray tube which employs magnetic deflection. The correct schematic symbol for a CRT employing electromagnetic deflection, is shown in Figure 3a.

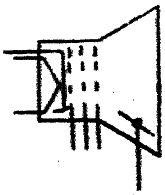
22. (Continued)



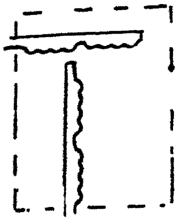
a b

Figure 3

The schematic symbol in figure 3b shows electrostatic deflection. The difference between the two can be seen by comparison. The symbol for an electrostatic CRT shows the deflection plates  but the symbol for an electromagnetic CRT shows neither the coils employed nor any type of plates used. The reason for this is that the deflection coils are normally shown at another place. By looking on sheet 2 of 2, the deflection coils (L1) may be found.

P.I.	
	22. (Contineud) The schematic symbol of a CRT employing electromagnetic deflection ________ (will/will not) show the deflection coils with the symbol.
will not	23. Draw the schematic symbol of a CRT employing electromagnetic deflection.
	24. Draw the schematic symbol for the coils in an electromagnetic deflection system.

P.I.



25. The function of the "X" and "Y" yoke driver feedback signals is to

a. keep the deflection coils from being overdriven.

b. provides a constant conduction level in the sweep processor differential amplifier.

c. provide a test point for the final sweep signal.

d. provide degenerative feedback to the sweep processor differential amplifier.

e. reduce the conduction level in the sweep processor differential amplifier.

---

d.

26. The sweep on the face of a plan position indicator will rotate in synchronization with the antenna as it rotates through 360 degrees of scan. The sweep sawtooth currents are resolved, as shown in figure 4a, b, c, and d, by the sweep resolver in the antenna unit. The "X" sweep sawtooth currents are maximum in amplitude at 90° and 270° and minimum at 0° and 180°.

The "Y" sweep sawtooth currents are maximum at 0° and 180° and minimum at 90° and 270°. This analysis shows that the "X"

26. (Continued)

and "Y" sweep currents are 90° out of phase and the amplitude varies at a sinusoidal rate.

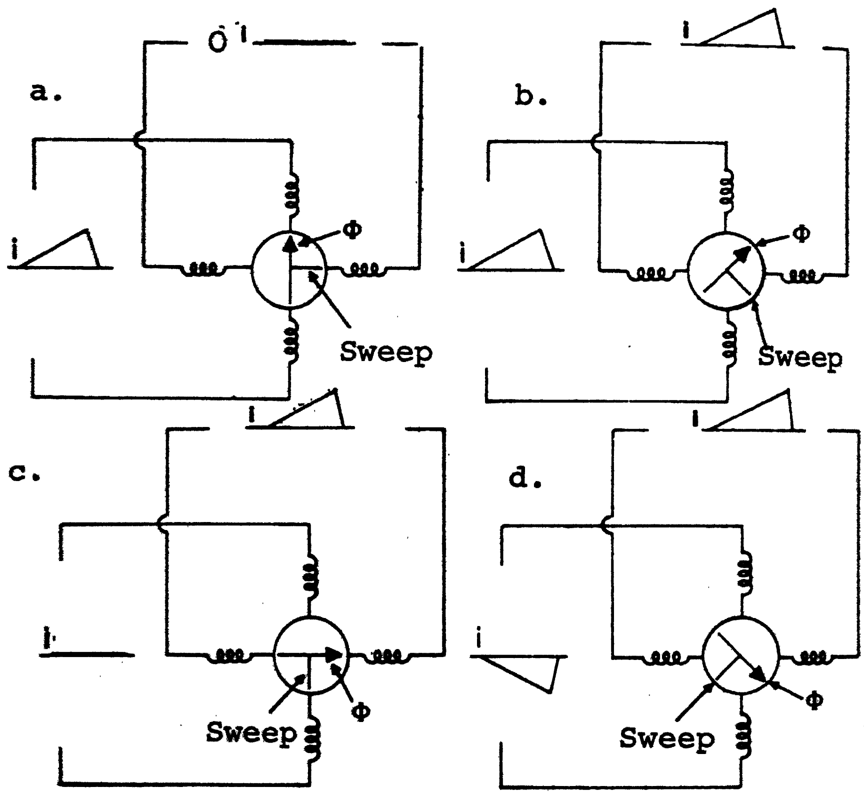
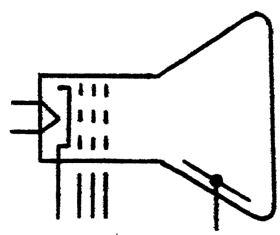


Figure 4

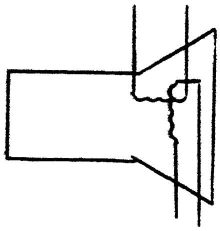
The sweep currents applied to the deflection coils are ____________ out of phase and vary in amplitude at a sinusoidal rate.

P.I.	
90°	27. The signals applied to the deflection coils that cause the sweep rotation are a. a sweep voltage varying at a sinusoidal rate. b. two sweep voltages 180 degrees out of phase varying at a sinusoidal rate. c. two sweep currents 90 degrees out of phase varying at a sinusoidal rate. d. a sweep current in phase, varying at a sinusoidal rate.
c.	28. The schematic symbol below is the correct symbol for a CRT employing electromagnetic deflection. TRUE/FALSE 

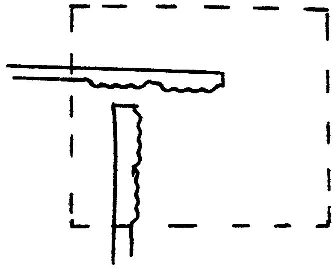
TRUE

29. The schematic symbol used to represent the electromagnetic deflection coil is

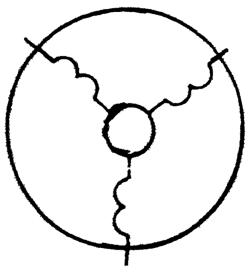
a.



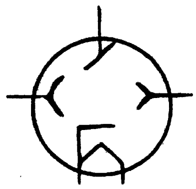
b.



c.



d.



P. I.

b.

30. In figure 5a, a sweep current, I, is applied to the horizontal deflection coils only, and the resulting magnetic field lies along the axis of the coils. The sweep is horizontal because the electron beam is deflected perpendicular to the magnetic field. In figure 5b, sweep currents are applied to both sets of coils, and the resultant magnetic field takes a position between the axis of the two sets of coils.

NOTE: Because of this shift in the magnetic field, the sweep is rotated clockwise from its original position. The two current waveforms are exactly alike and are applied simultaneously.

In figure 5c, sweep current is applied to the vertical coils only, and the sweep lies 90 degrees clockwise from its original position. Further rotation is obtained if the phase of the deflection coil currents are reversed, as illustrated in d and e.

30. (Continued)

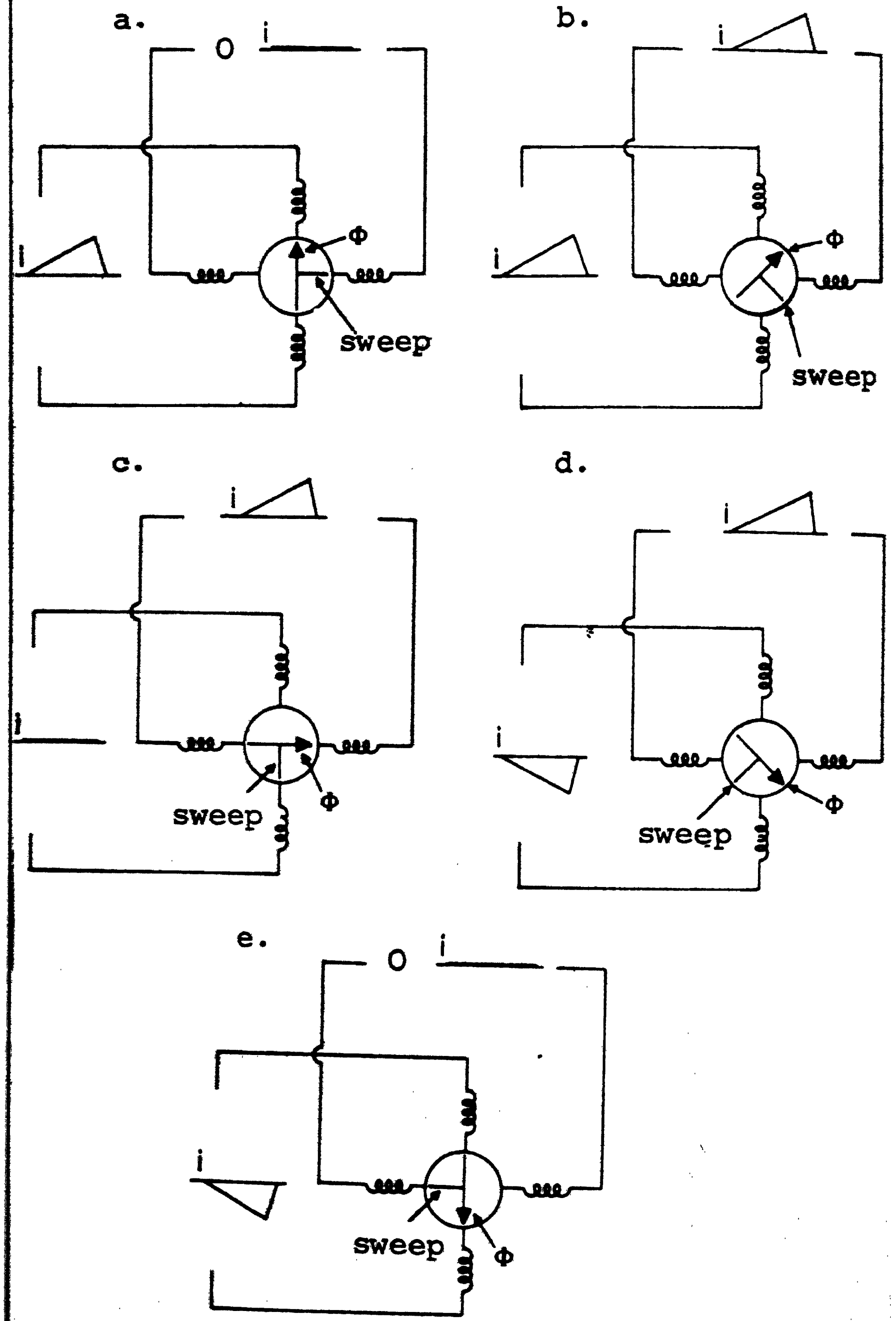


FIGURE 5

P.I.

30. (Continued)

Figure 6 illustrates the resultant currents produced by the rotating sweep. The deflection envelopes are sinusoidal and have a cycle time equal to one complete rotation of the radar antenna. The signal envelopes differ in phase by 90 degrees and have equal peak values. Individual sawtooth waves of current are applied to the deflection coils simultaneously; the phase difference of 90 degrees applies only to the variations of amplitude from one sawtooth to the next.

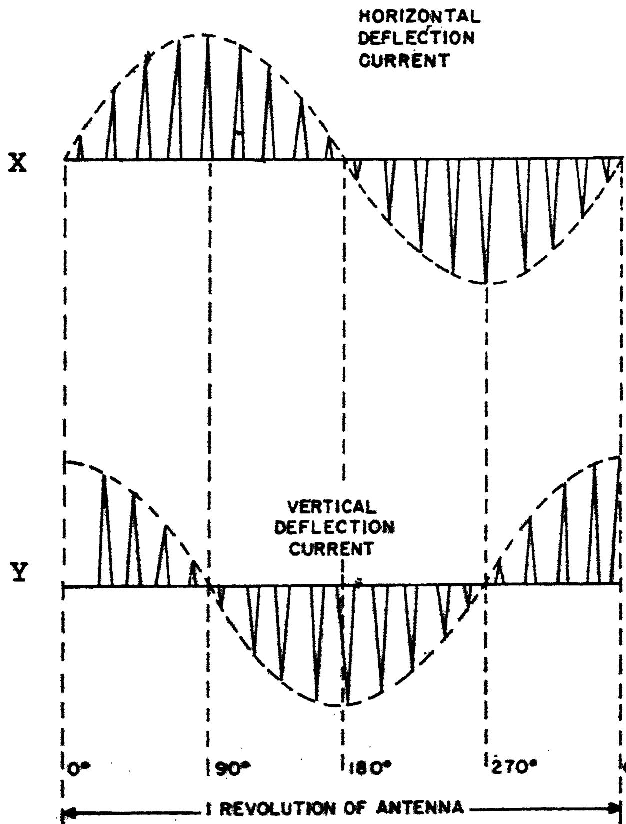


Figure 6

P.I.

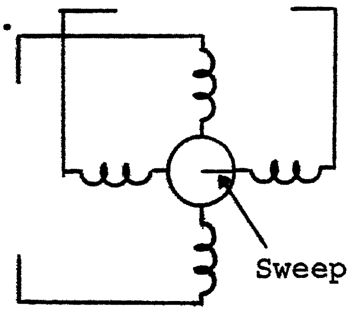
30. (Continued)

The sweep deflects from the center to the right-hand edge when the X sweep is maximum positive and the Y sweep is __________.

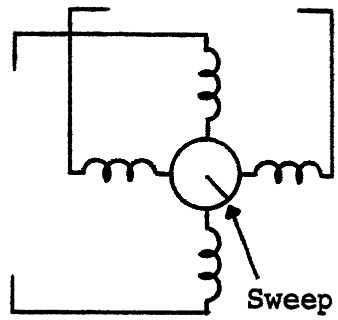
Zero

31. Which two of the below diagrams show the correct sweep deflection if the sweep current is applied to the "X" deflection coils only?

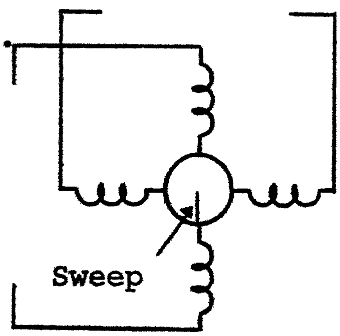
a.



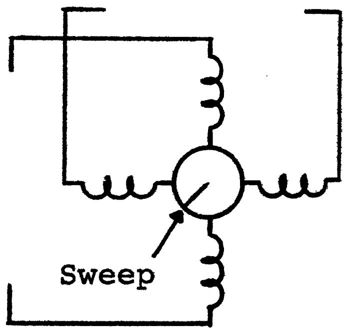
b.



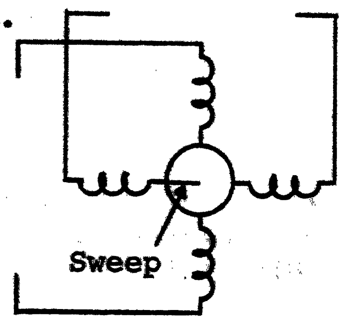
c.



d.

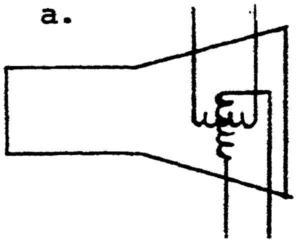


e.

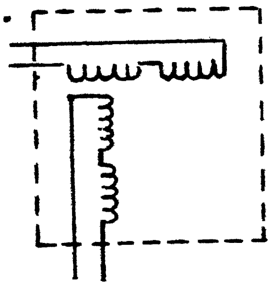


P.I.	
a, e	32. Two sweep currents, 90 degrees out of phase and varying in amplitude at a sinusoidal rate, are applied to the deflection coils and cause the ______________ ____________ to occur.
sweep rotation	33. Which of the below is the schematic symbol for a CRT which uses electromagnetic deflection?

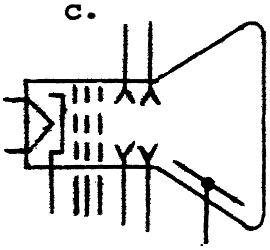
a.



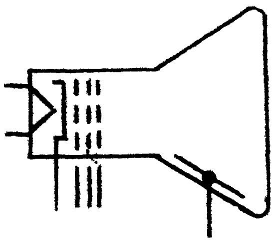
b.



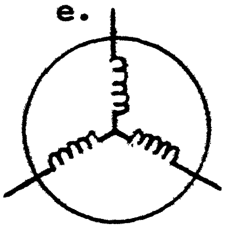
c.



d.



e.



d.	34. When the direction of the sweep deflection is along the horizontal plane, the sweep current is applied to the ______ (X/Y) deflection coils.
X	35. The signals applied to the deflection coils that cause the sweep rotation in a PPI scope are a. two sweep currents, in phase, varying at a sinewave rate. b. two sweep currents, 90 degrees out of phase, varying at a sinewave rate. c. a sweep voltage which varies at a sine wave rate. d. a sweep current which varies at a sine wave rate.
b.	36. Select two directions the electron beam may be deflected when the sweep current is applied to the "X" deflection coils only. a. Upward b. To the left. c. To the right. d. Downward.

P.I.	
b, c	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 6

GATED COLPITTS OSCILLATOR

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-6

GATED COLPITTS OSCILLATOR

In this lesson topic, you will study the input network and gated Colpitts oscillator circuit configuration, purpose, and operation. A laboratory assignment will reinforce the explanation of the oscillator operation in the range marks generator card.

The learning objectives for this lesson topic are as follows:

1. Given a list of circuits, select the input network to the gated Colpitts oscillator on the range marks generator card.

2. Select from a list, the statement that describes the purpose/operation of the input network to the gated Colpitts oscillator.

3. Given a list of statements, select three that describe the gated Colpitts oscillator used on the range marks generator card.

4. Given a list of statements, select two that describe the purpose/operation of Q1 in the Colpitts oscillator.

5. Select from a list, the statement that describes the purpose/operation of R3 and R6 in the collector circuit of the Colpitts oscillator.

6. Select from a list, the statement that describes the purpose/operation of L1, C7, and C8 in the Colpitts oscillator on the range marks generator card.

*7. Given an Airborne Search Radar System Trainer, its MIM and appropriate test equipment, measure and record voltages and waveforms at specified test points on a gated Colpitts oscillator and input logic network.

NOTE: All objectives in this lesson topic must be accomplished with 100% accuracy, unless otherwise stated.

* Accomplished in lab.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-6

GATED COLPITTS OSCILLATOR

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job program in Job Program Booklet.
2. Student response sheets.
   a. Job Data Sheet.
   b. Answer sheet for use with test.
   c. Programmed instruction response sheets.

ENRICHMENT MATERIALS:

1. MIM, 15A21.
2. Basic Electronics, Vol. I, NAVPERS 10087-C, Chapter 15.

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

GATED COLPITTS OSCILLATOR

INTRODUCTION

You have studied many types of oscillators. This lesson topic covers the Gated Colpitts Oscillator on the range marks generator card in the synchronizer. You will study the circuit configuration and its use as a range mark generator. The study of this oscillator will be continued in a laboratory assignment by means of a voltage and waveform analysis. Within the synchronizer unit (A3) are the cards controlling the sweep sawtooth, sweep gates, and range marks. The sweep sawtooth and gates have already been covered in lesson topics 5-5-1 and 5-5-2. Refer to the schematic diagram of the range marks generator card (A3A3).

1. The positive sweep gate, from the Sweep Generator Card, is applied to the Range Marks Generator Card to control the generation of the range marks. The leading edge of the positive sweep gate represents time zero (T0) or the start of the sweep sawtooth. This signal is applied to the dual inverter U1 (see figure 1). The positive sweep gate is felt on U1A, pin 9, inverted at pin 8, and applies to U1B, pin 5, where

P.I.

1. (Continued)

the sweep gate is inverted a second time, and it again appears as a positive sweep gate at U1B-6. The width of the positive gate is dependent on the selected range.

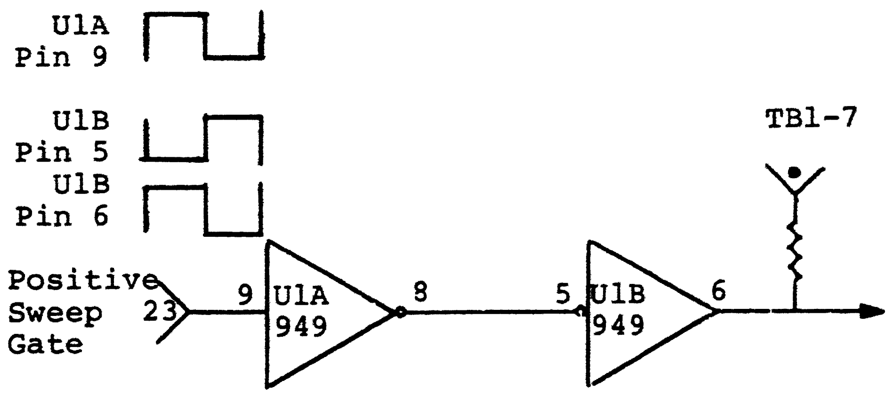


Figure 1 - DUAL INVERTER, U1.

The input network to the gated Colpitts oscillator is a dual ________________ ,U1.

P. I.	
inverter	2. The dual inverter, U1, is the a. sweep gate generator. b. range marks Colpitts oscillator. c. gated Colpitts input network. d. range marks gate.
c.	3. During the operation of the range marks generator, the input network will provide coupling of the positive sweep gate to the oscillator. The amplitude of the output is the same as the input. The dual inverter, U1 A & B, also provides isolation of the oscillator to prevent the oscillator from affecting the sweep gate generator circuit. The input network to the gated Colpitts oscillator is a dual inverter that ________________ the positive sweep gate to Q1 and ____________ the Colpitts oscillator.

P. I.	
couples	4. The purpose of the dual-inverter U1 A & B is to: a. amplify the positive sweep gate. b. couple and positive sweep gate and isolate the Colpitts oscillator. c. couple the Colpitts oscillator output and isolate this from the sweep gate generator circuit. d. double invert the positive sweep gate before applying it to the range mark pulse generator.
b.	5. The positive sweep gate is applied to the range marks generator card to gate the development of range marks. The positive sweep gate is applied to the Colpitts oscillator through a ______________ ______________________________.
dual inverter	6. Refer to figure 2. Q1 and its associated circuitry on the range marks generator card make up the gated Colpitts oscillator. The oscillator is made up of transistor Q1 and a parallel tank in the base circuit. The feedback to sustain the oscillations is applied to capacitors C7 and C8 from the emitter of Q1. The output of

6. (Continued)

the oscillator is also taken from the emitter of Q1 through C5, R10, and R15.

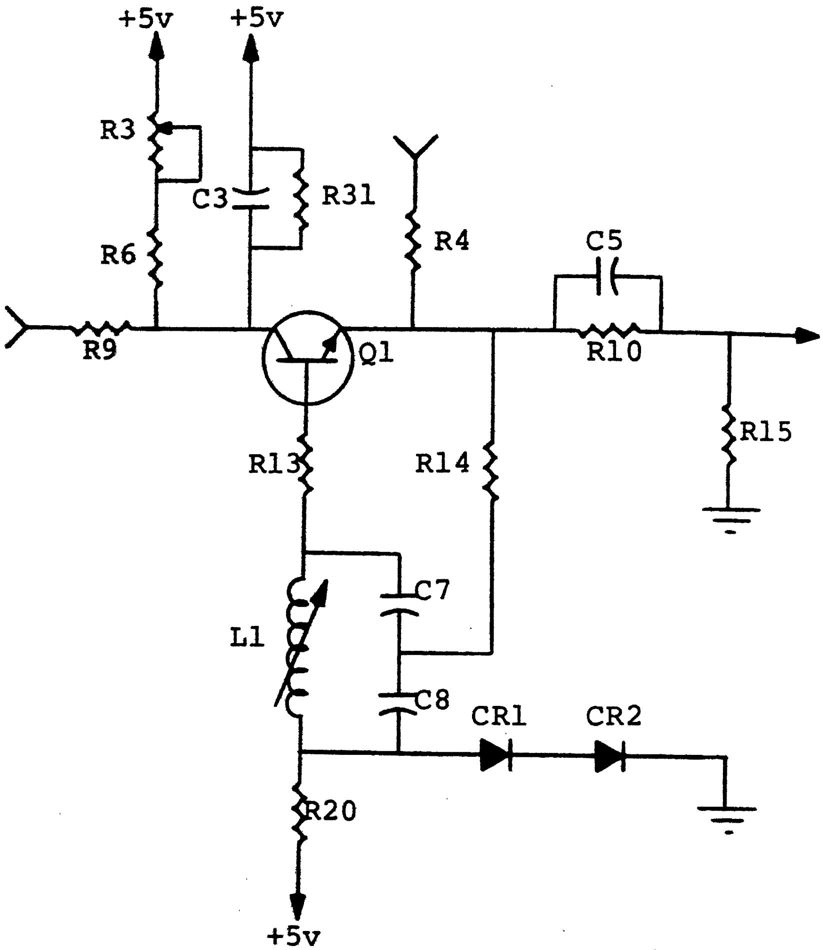


Figure 2 - SCHEMATIC OF GATED COLPITTS OSCILLATOR

The Colpitts oscillator uses transistor Q1 with a ____________ tank in the base circuit. The output and __________ are provided by the emitter circuitry.

P.I.	Module 5-5 Lesson Topic 5-5-6
parallel feedback	7. Select three statements that describe the gated Colpitts oscillator. a. It uses transistor Q1 with a parallel tank in the base circuit. b. The output is taken from pin 3 of U2. c. The output is taken from the emitter of Q1. d. The oscillator tank uses a dual capacitor, dual inductor configuration. e. Feedback to the dual capacitor tank. is taken from the emitter of Q1.
a, c, e.	8. The purpose of the input network of the range marks generator is to ____________ the Colpitts oscillator from the input and ____________ the positive sweep gate.
isolate couple	9. Refer to the schematic diagram of the range marks generator card. The input network to the gated Colpitts oscillator is a a. push-pull amplifier, Q3 and Q4. b. dual inverter, U1. c. three-step logic counter, U3. d. level comparator, U2.

b.

10. Refer to the schematic diagram of the Range Marks Generator Card. Transistor Q1 operates as a gated, 81-kHz, sine wave Colpitts oscillator. Between sweep gates, when the gate at U1, pin 6, is low (negative), the U1 side of R9 is effectively at ground. The voltage drop across potentiometer R3 and resistor R6 is sufficient to remove the collector voltage from Q1. When the gate goes high (positive) at U1, pin 6, approximately 5 vdc is applied to the collector side of resistor R9 for the duration of the gate. During the period of the positive gate, collector voltage is restored to Q1, causing conduction, and the circuit will oscillate at approximately 81 kHz. The oscillations generated by the tank circuit during the positive gate are applied from the junction of L1 and C7 through R13 to the base of Q1. Q1, operating as a class A amplifier, amplifies the oscillations and the output is taken from the emitter. The emitter output is in phase with the base and is returned to the tank circuit as <u>regenera-</u>

P.I.	Module 5-5 Lesson Topic 5-5-6
	10. (Continued) <u>tive</u> feedback. The feedback is used to sustain oscillations in the tank circuit during the positive gate. Transistor Q1 in the gated Colpitts oscillator ____________ the oscillations from the tank circuit and applies __________ ____________ to the tank circuit to sustain oscillations.
amplifies regenerative feedback	11. Which component in the gated Colpitts oscillator amplifies the tank oscillations and applies a regenerative feedback signal to the tank circuit? a. U1. b. C1. c. Q1. d. L1.
c.	12. The transistor, Q1, in the 81 kHz gated Colpitts oscillator utilizes a __________ __________ in the base circuit and the emitter circuit provides both an ____________ and regenerative ______________ to the tank circuit.

parallel tank output feedback	13. Refer to the schematic diagram of the range marks generator card. The input network to the Colpitts oscillator is a. an amplifier used for gain. b. a down counter used for frequency dividing. c. a dual inverter that couples the positive sweep gate to Q1 and isolates the Colpitts oscillator. d. A triple inverting logic gate used to phase-invert the input signal without amplification.
c.	14. Refer to the schematic diagram of the Range Marks Generator Card. Potentiometer R3 and resistor R6 make up the collector load resistance. The variable resistance in the collector circuit is used to shift the start of the first oscillation (which occurs too close to time zero) so that the range marks will occur at the proper time on the sweep waveform. The shifting of this first oscillation is performed by changing the <u>dc</u> <u>reference</u> voltage felt on the collector of Q1. This change in collector voltage has <u>no</u> effect on the amplitude of the oscillations.

P.I.	
	14. (Continued) R3 and R6 form a collector load resistance and establish the dc ____________ of the oscillations.
reference	15. The components that determine the dc reference of the oscillations are: a. C3 and R31. b. R3 and R9. c. R4 and R15. d. R6 and R3.
d.	16. Q1 in the Colpitts oscillator is used to ______________________ the tank oscillations and provide __________ _______________ to the tank circuit.

P. I.	
amplify regenera- tive feedback	17. Refer to the schematic diagram of the range marks generator card. Select the statements that describe the gated Colpitts oscillator. a. The Colpitts oscillator uses transistor Q1 with a parallel tank in the base circuit. b. Feedback to the dual capacitor tank is taken from the emitter circuit. c. Output of the oscillator is taken from the emitter of Q1. d. Output of the oscillator is taken from pin 3 of U2. e. Oscillator tank uses dual inductor configuration.
a, b, c.	18. Refer to the schematic diagram of the Range Marks Generator Card. The tank circuit in the base of Q1 consists of variable inductor L1, and capacitors C7 and C8. This tank circuit is adjusted for approximately 81 kHz. The frequency of 81 kHz is used as the basic timing reference because one complete cycle is approximately 12.36 microseconds or equivalent to approximately one radar range mile. During the oepration of the Colpitts oscillator, the tank circuit oscillations

P.I.	
	18. (Continued) will continue because of regenerative feedback until the input positive gates change to the low state, cutting off transistor Q1. When the circuit starts operation, capacitors C7 and C8 will charge and the resultant current flow will establish a magnetic field around L1. When the capacitors complete their charge, the field around L1 will collapse establishing the circulating current in the tank. The oscillations produced will continue until Q1 is cut off by the negative pulse width of the positive sweep gate input. L1, C7, and C8 form a _____________ tank to produce the 81 kHz sine waves.
parallel	19. The parallel tank circuit is made up of components a. R13. b. L1. c. R20. d. C5 and R10. e. C7 and C8.

P.I.	
b, e.	20. Referring to the schematic diagram of the Range Marks Generator Card, the purpose of R3 and R6 in the collector circuit of Q1 is to establish the ____________ ________ of the oscillations.
dc reference	21. Refer to the Range Marks Generator Card schematic diagram. Q1 in the Colpitts oscillator circuit is used a. to phase-invert the input squarewave. b. to provide feedback to the tank circuit. c. to amplify the oscillations from the tank circuit. d. as a saturation limiter to hold the input signal at a fixed amplitude.
b, c.	22. The purpose of L1, C7, and C8 in the Colpitts oscillator is to form a __________ ____________ to produce ____________ kHz sine waves.

P.I.	
parallel tank 81	23. Refer to the schematic diagram of the Range Marks Generator Card. Select the statement that describes the purpose/ operation of R3 and R6 in the Colpitts oscillator. a. Current limiting resistors to protect Q1. b. Collector load resistance for Q1 and determine the dc reference of the oscillations. c. During the negative portion of the input pulse, R3 and R6 form a discharge path for C3 to hold Q1 cutoff. d. R3, R6, and C3 form a band reject circuit to block all unwanted frequencies.
b.	24. Refer to the schematic diagram of the Range Marks Generator Card. Select the statement that describes the purpose of L1, C7, C8 in the Colpitts oscillator. a. L1, C7, and C8 are used to compensate for bias changes due to temperature changes. b. C7 and C8 produce opposite discharges to prevent ringing in L1 at cutoff. c. L1 provides an inductive kick to double the output voltage of C7 and C8 at the collector of Q1. d. L1, C7, and C8 form a parallel tank to produce the 81 kHz sine wave.

d. At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 7

CIRCUIT ANALYSIS OF VOLTAGE DOUBLERS AND BLEEDER CIRCUITS

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-7

CIRCUIT ANALYSIS OF VOLTAGE DOUBLERS AND BLEEDER CIRCUITS

This lesson topic will present the configuration, schematic representation, and operation of the half-wave and full-wave voltage doubler circuits and the high voltage bleeder circuits employed in radar systems.

The learning objectives for this lesson topic are as follows:

1. Select from a list the schematic diagram of a half-wave voltage doubler.

2. Given a list of statements, select two that describe the function of circuit components in the half-wave voltage doubler.

3. Given a list of statements, select three that describe the operation of the half-wave voltage doubler.

4. Select from a list the schematic diagram of a full-wave voltage doubler.

5. Select from a list two statements that describe the function/operation of circuit components in the full-wave voltage doubler.

6. Given a list of statements, select three that describe the purpose of the bleeder network.

7. Select from a list two statements that describe the bleeder circuit configuration and operation.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-7

CIRCUIT ANALYSIS OF VOLTAGE DOUBLERS AND BLEEDER CIRCUITS

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

Student Response Sheets.

a. Answer sheet for use with test.
b. Programmed instruction response sheets.

ENRICHMENT MATERIAL:

Basic Electronics, Vol. I, Ch. 5, pages 99-101, NAVPERS 10087-C.

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PROGRAMMED INSTRUCTION

CIRCUIT ANALYSIS OF VOLTAGE DOUBLERS AND BLEEDER CIRCUITS

INTRODUCTION

It has been shown in an earlier lesson that is is possible to get a high voltage out of a simple half-wave rectifier provided the load current is low. If the current demand is high, the output voltage will decrease. In the simple half-wave rectifier (FIGURE 1) the charge time for the circuit is very short since the capacitor's charge path is through the diode CR1, surge resistor R, and the secondary of the transformer.

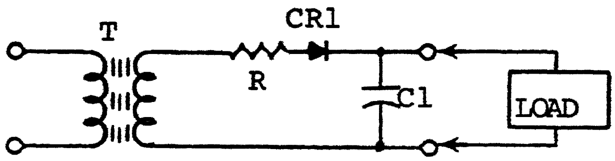


FIGURE 1 - SIMPLE HALF-WAVE RECTIFIER USED TO DELIVER INCREASED VOLTAGE OUTPUT.

The combination of these elements form a very low impedance during the charge time. In comparison, the discharge path for the capacitor is through the load which offers an impedance several hundred times higher than the charge path. The lower the load impedance, the greater the current. If the discharge path for the capacitor offers a lower impedance, the capacitor will discharge more, lowering the output voltage.

Half-wave and full-wave rectifier circuits that can be used to double the input voltage will now be discussed. All these circuits have one thing in common - they sum the charge stored by the capacitors.

1. The first voltage doubler is the half-wave voltage doubler. As the name implies, this circuit provides a dc voltage output that is approximately twice that obtained from equivalent half-wave rectifier circuit.

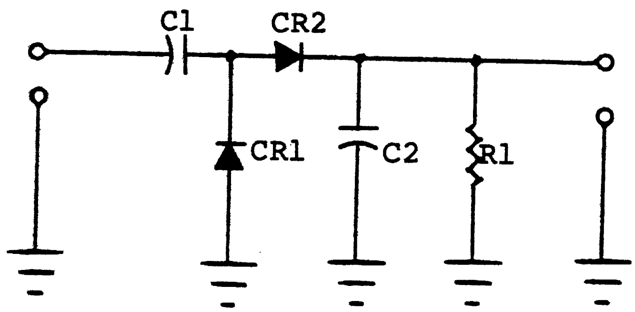


FIGURE-2: HALF-WAVE VOLTAGE DOUBLER

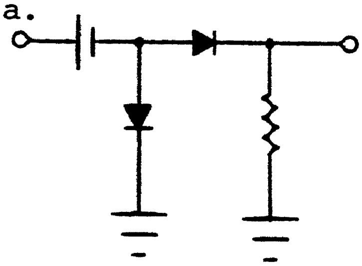
Figure 2 shows the schematic for a typical half-wave voltage doubler circuit. The output voltage is positive with respect to ground, it could just as well operate as a negative voltage doubler by reversing the diodes.

P.I.

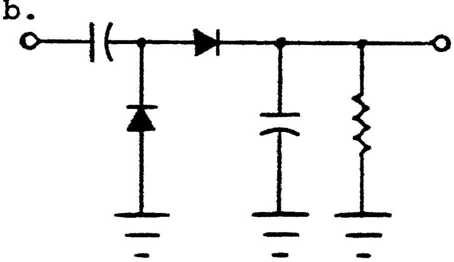
1. (Continued)

Which of the following schematics is a half-wave voltage doubler?

a.



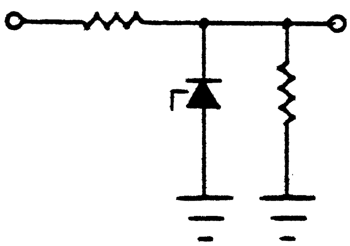
b.



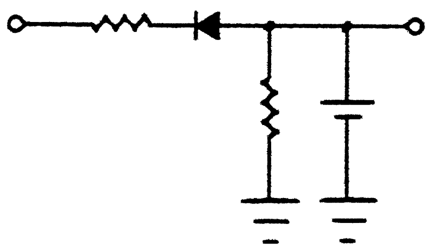
b.

2. Which schematic represents a half-wave voltage doubler?

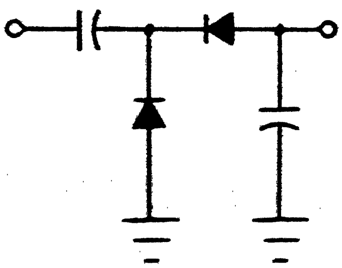
a.



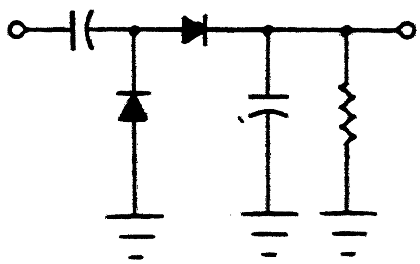
b.



c.



d.



P.I.

d.

3. Refer to figure 3. The function of CR1 is to provide a charge path for C1. The function of CR2 is to provide a discharge path for C1 and a charge path for C2.

When C1 is discharged through CR2 the voltage stored by C1 aids the charge of C2. C2 stores a charge of twice the input voltage and from it the output voltage is taken. Bleeder resistor R1 is used to discharge C2 when power is removed.

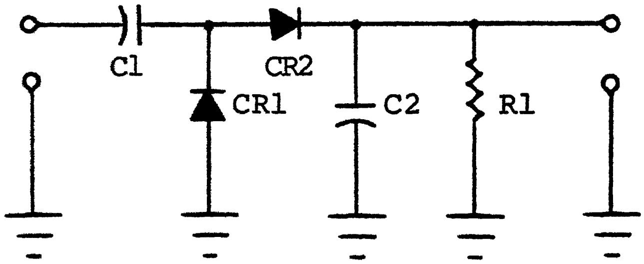


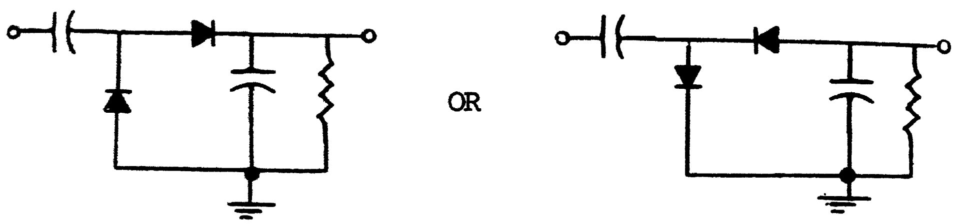
FIGURE 3 - HALF-WAVE VOLTAGE DOUBLER

The diodes provide __________ paths for C1 and C2.

C1 ______________ the charge on C2, which is the output voltage. Bleeder resistor R1 ____________ C2 when power is removed.

charge aids discharges	4. Select the statement that correctly describes the function of the components in a half-wave voltage doubler. a. CR1 and CR2 provide charge paths for the capacitors and C1 aids the charge of C2 which increases the output voltage. Bleeder resistor R1 discharges C2 when power is removed. b. CR1 provides the discharge path for C2 and CR2 provides for the charge of C2, doubling the output voltage. c. C1 and C2 charge in parallel through diodes CR1 and CR2.
a.	5. Draw a half-wave voltage doubler circuit in the space below.

5. (Continued)



6. Refer to Figure 4 below. In the operation of the half-wave voltage doubler, an ac sine wave (0 volt reference) is applied to C1.

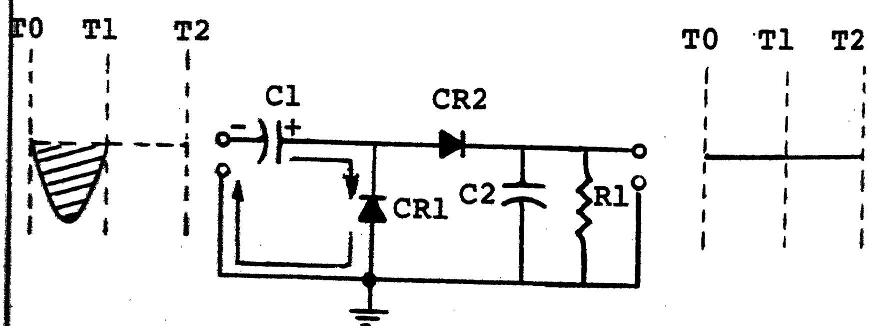


Figure 4a

P.I.

6. (Continued)

When the input signal is negative (T0 to T1), CR1 conducts and C1 charges to the peak of the negative alternation, as indicated by the polarity symbols. At this time there is no output voltage from the circuit. Refer to figure 4b below. When the input signal goes positive (T1 to T2), CR2 conducts providing a charge path for C2. The charging of C2 is aided by the charge already on C1, and C2 will charge to approximately twice the peak of the input voltage.

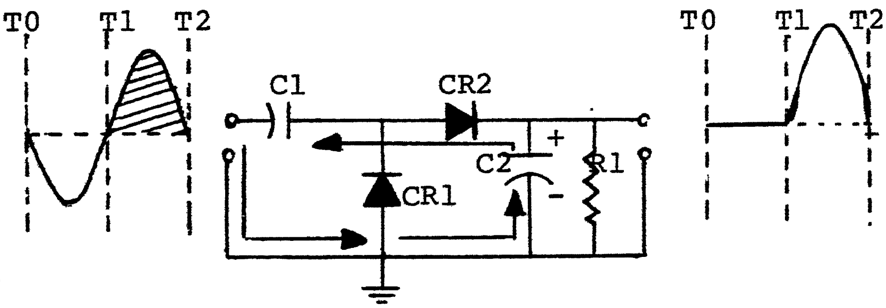


Figure 4b

This action will continue during subsequent cycles of the input waveform. Also, as in the half-wave rectifier, C2 will attempt to discharge slightly through R1 during each negative alternation of the input. The amount C2 discharges during the negative alternation will affect the amount of ripple present in the dc output voltage. Once power is removed bleeder resistor R1 discharges C2.

6. (Continued)

After the input signal has been applied for several cycles, C1 charges during each ___________ half cycle and C2 charges, with C1 aiding the input, during the _____________ half cycle. During each succeeding negative half cycle, C2 _____________ slightly.

negative
positive
discharges

7. Which statements correctly describe the operation of a half-wave voltage doubler circuit? (Select three)

a. During the negative half cycle C1 charges.

b. C1 filters the ac component of the input signal.

c. C2 charges, with the aid of C1, to produce a doubled output voltage, during the positive half-cycle.

d. During the negative half-cycle C2 attempts to discharge through R1.

e. During the positive half-cycle C2 charges to the potential on C1.

P.I.

a,
c,
d.

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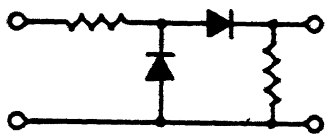
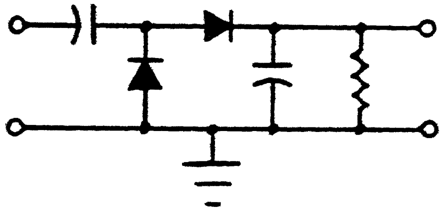
8. The function of the diodes CR1 and CR2 is to provide the ____________ __________ for C1 and C2. C1 ________________________ the charge of C2, and the charge on C2 is the output voltage.

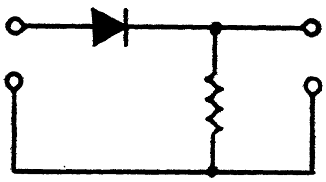
charge paths

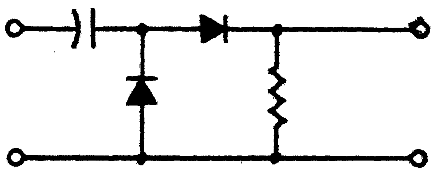
aids

9. Which of the following schematics represent a half-wave voltage doubler?

a.


b.


c.


d.


b.

10. Another kind of voltage doubler is the FULL-WAVE VOLTAGE DOUBLER. (Refer to Figure 5 for circuit schematic.)

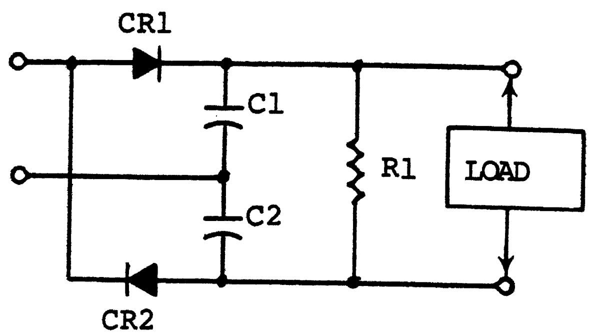


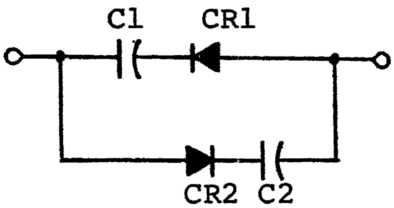
FIGURE 5 - FULL-WAVE VOLTAGE DOUBLER

The circuit operates much the same as the full-wave rectifier with the exception that now two capacitors are employed. Each capacitor is charged to approximately the peak voltage of the input and the charges are added together to provide a single output.

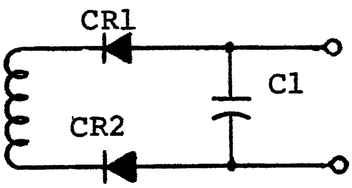
The full-wave voltage doubler utilizes ____________ ________________. The charges are added together to provide a single output.

a full-wave voltage doubler?

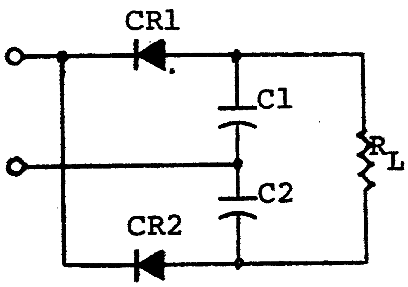
a.



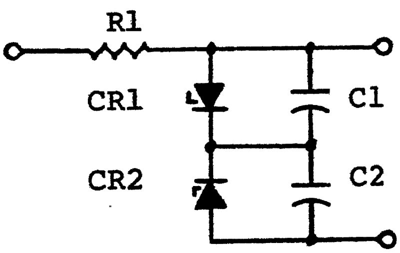
b.



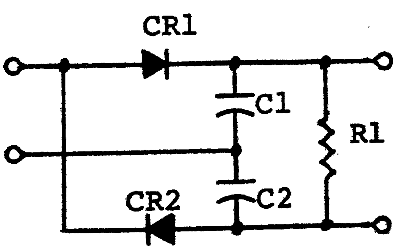
c.



d.



e.



P.I.

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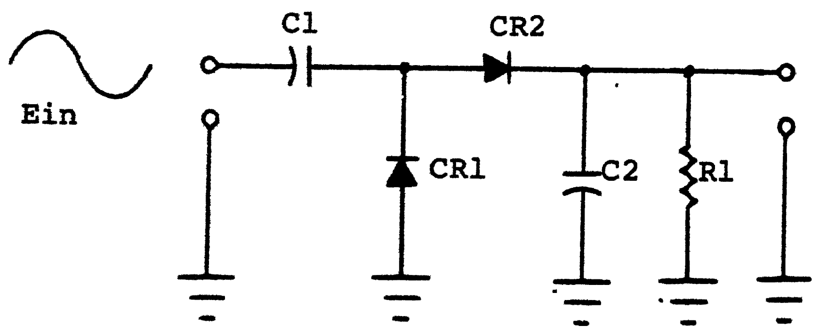
e.

12. Refer to the schematic diagram of the half-wave voltage doubler below and assume that the input has been applied for several cycles.

During the negative half-cycle, ________ (C1/C2) will charge and ________ (C1/C2) will attempt to discharge through R1. During the positive half-cycle, ________ (C1/C2) charges, aided by the charge on ________ (C1/C2) to produce a doubled output voltage.



P.I.	
C1, C2, C2, C1.	13. The functions of the circuit components in the half-wave voltage doubler are: a. CR1 and CR2 are used for current reduction. b. The charge on C1 aids the charge on C2 and the charge on C2 is the output voltage. c. C1 opposes C2 to prevent C2 from discharging. d. CR1 and CR2 provide charge paths for C1 and C2.
b, d.	14. The full-wave voltage doubler operates much the same as the full-wave rectifier. Figure 6 is an illustration of the full-wave voltage doubler. When the a-c input voltage is positive at point "A" with respect to point "B", C1 will charge to nearly the peak value of the positive alternation through CR1. The polarity of the charge across C1 is indicated by the polarity signs.

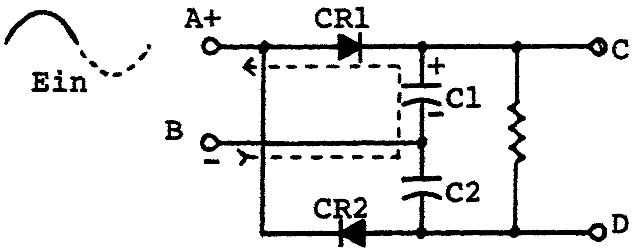


FIGURE 6

P.I.

14. (Continued)

Figure 7 illustrates the operation of the full-wave voltage doubler circuit during the negative alternation of the input a-c. In this illustration point "A" is negative with respect to point "B". Conduction is through CR2 and C2 will charge to nearly the peak of the negative alternation of the a-c input. The charge across C2 is indicated by the polarity signs.

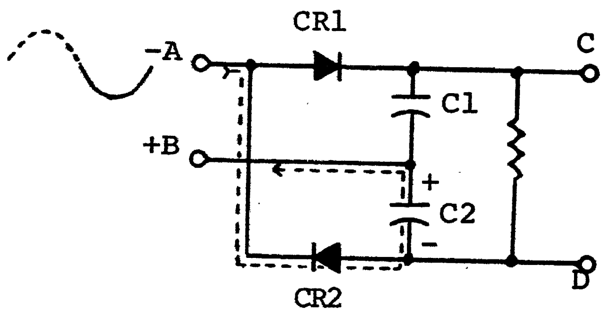


FIGURE 7

Figure 8 depicts the voltage applied to the load. Notice the polarity signs across C1 and C2; the value of voltage applied to the load is equal to the sum of the voltages across C1 and C2 because they discharge in series and are in parallel with R1 and the load.

P.I.

14. (Continued)

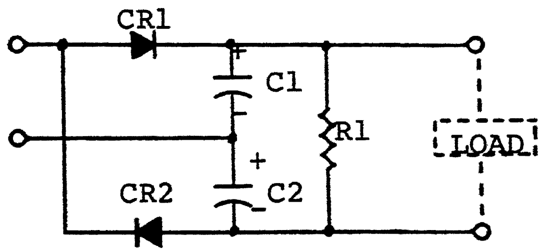
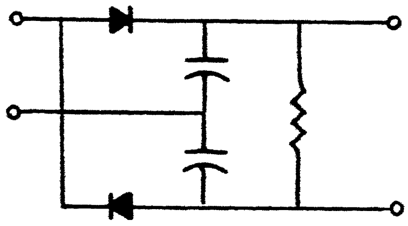


FIGURE 8

In a full-wave voltage doubler CR1 and CR2 provide ______________ paths for C1 and C2. The capacitors will ______________ independently and ________________________ in series to produce the doubled voltage across the load. Bleeder resistor R1 provides a discharge path for the capacitors when power is removed.

P.I.	
charge charge discharge	15. Three functions/operations of the circuit components in a full-wave voltage doubler are: a. CR1 and CR2 provide charge paths for C1 and C2. b. C1 and C2 charge independently and discharge in series to produce the doubled voltage output. c. CR1 and CR2 limit the input to prevent over-charging of the capacitors. d. C1 and R1 form a coupling circuit. e. C2 and R1 form a differentiator. f. Bleeder resistor R1 is used to provide a discharge path for the capacitors when power is removed.
a, b, f.	16. Draw the circuit schematic for a full-wave voltage doubler in the space below.

16. (Continued)



17. Select three statements that describe the operation of the half-wave voltage doubler.

a. During negative half-cycles C1 charges.

b. C1 filters out voltage charges.

c. During positive half-wave cycles C2 charges, with the aid of C1, to produce a doubled voltage output.

d. During positive half-cycle C2 charges to the potential of C1.

e. During negative half-cycles C2 attempts to discharge through R1.

P.I.	
a, c, e.	The output of a power supply can be applied to some loads that will retain a high voltage long after the equipment has been turned off. This is especially true when the load is a CRT in a TV set, an oscilloscope, or a radar display indicator. The CRT can retain a voltage charge that is harmful and can be fatal. A bleeder resistor can be connected in parallel with the load. While the equipment is turned off, the bleeder resistor will provide a discharge path for the charge. This reduces the voltage to a low value, thereby reducing the hazard. NO RESPONSE REQUIRED

P.I.	
	  SAFETY NOTE ALTHOUGH BLEEDER NETWORKS ARE MEANT TO REDUCE SHOCK HAZARD, THEY DO NOT ELIMINATE THE POSSIBILITY OF A HARMFUL OR FATAL ELECTRICAL SHOCK. ALWAYS MAKE SURE THAT A CRT HAS BEEN FULLY DISCHARGED BEFORE WORKING ON OR AROUND IT.
	18. Refer to figure 5-11 in the MIM. The high voltage power supply (A4PS1) provides a coarsely regulated high voltage (7 KV) at a low current level to be used to supply the second anode of the CRT. This output is applied to a chain of bleeder resistors (R1 - R16). The voltage drop across R17 (TP9) can be measured to assure that the output of the power supply is the proper value. The voltage measured at TP9 should be +100vdc. The bleeder network provides a constant load for the 7 KV power supply and a discharge path for the filter network of the high voltage power supply when the radar set is turned off.

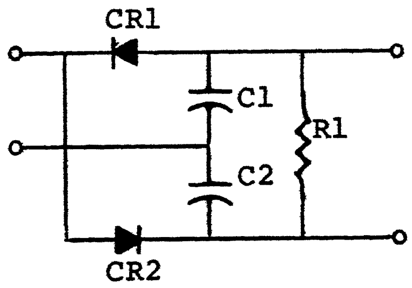
P.I.

18. (Continued)

SAFETY NOTE

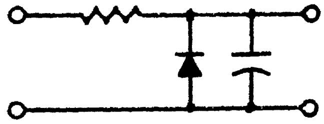
BECAUSE OF THE HIGH VOLTAGE PRESENT IN THE BLEEDER NETWORK AND IN THE 7 KV POWER SUPPLY ALL SAFETY PRECAUTIONS MUST BE OBSERVED WHEN WORKING ON OR AROUND THESE CIRCUITS.

The bleeder network has three purposes within the display indicator: it provides a ______________ path for the 7 KV power supply when the radar is turned off, it provides constant ______________ for the 7 KV power supply, and it provides a representative voltage of __________vdc at TP-9 to assure the power supply is within tolerance.

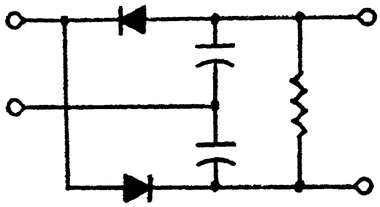
P.I.	Module 5-5 Lesson Topic 5-5-7
discharge load +100	19. Select three purposes of the bleeder network in the display-indicator. a. Constant load for the 7 KV power supply. b. Provides a charge path for the 7 KV power supply. c. Provides a discharge path for the 7 KV power supply. d. Negative 100 vdc is at TP 9. e. Positive 100 vdc is at TP 9.
a, c, e	20. In the full-wave voltage doubler shown below, CR1 and CR2 provide ______________ ______________ for C1 and C2. C1 and C2 charge independently and ________________ in series to produce an output voltage ________________ the input voltage. 

21. Which of the following schematics represents a full-wave voltage doubler?

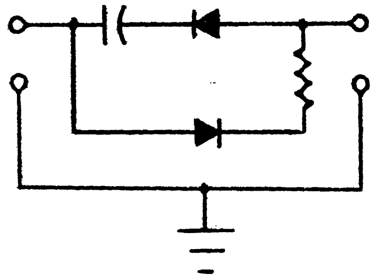
a.



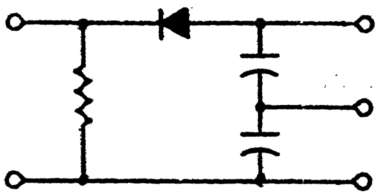
b.



c.



d.



P.I.	
b.	22. Figure 9 illustrates a voltage divider consisting of R1, R2, and R3. The lamps, DS1 and DS2, are the load resistances. One of the divider resistors has none of the load current flowing through it. This resistor is designated the bleeder resistor. (Figure 9).

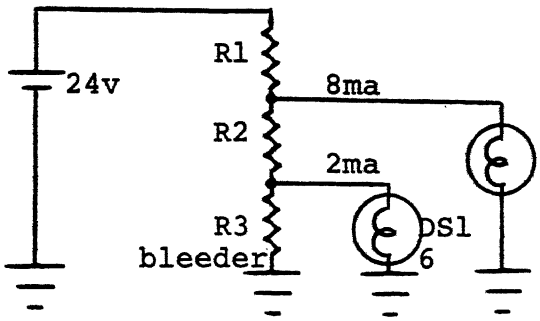


FIGURE 9

The bleeder resistor in figure 9 consists of one resistor, a bleeder network may consist of many resistors in series performing the same function as the single bleeder resistor. Refer to figure 5-11 (sheet 1 of 2) in the MIM. The resistors R1-R16 and R17 make up the bleeder network. These resistors are mounted on the A4A5 subassembly and act as a voltage divider network which provides a lower voltage that represents the 7 KV voltage applied to the CRT. This lower voltage can be measured at TP9.

P.I.	 22. (Continued) When the power is removed from the equipment the resistor network functions as a bleeder network to discharge the filter capacitors in the 7 KV power supply. The bleeder network consists of __________ connected in series that function as a __________ __________ while power is applied and as a __________ network while the power is off.
resistors voltage divider bleeder	23. Refer to the Radar Display Indicator assembly schematic. Which statements below describe the configuration and operation of the bleeder network? (Select two) a. The bleeder operates as a voltage multiplier. b. The bleeder operates as a voltage divider. c. Both parallel and series resistor combinations form the bleeder network. d. The bleeder is a parallel network of resistors. e. A simple series of resistors forms the bleeder network.

P.I.	
b, e.	24. When the radar system is in operation the bleeder network provides a ______________ load for the 7 KV power supply and voltage division to provide ________________ at TP-9. The bleeder network provides a ________________ path for the 7 KV power supply when the radar system is turned off.
constant +100vdc discharge	25. Select from the list below those statements that correctly describe the function of the components in a full-wave voltage doubler. (Select two.) a. C1 and R1 form a differentiator. b. CR1 and CR2 provide charge paths for C1 and C2. c. C2 and R1 provide bias voltage for CR2. d. CR1 and CR2 limit the input signal to prevent overcharging of the capacitors. e. C1 and C2 charge independently and discharge in series to produce the doubled output voltage.

P.I.	
b, e.	26. The bleeder network consists of a simple ________________ resistor network and operates as a ____________ ____________.
series voltage divider	27. From the list below, select three purposes of the bleeder network. a. Provides voltage doubling. b. Provides a discharge path for the 7 KV power supply when the radar is turned off. c. Provides voltage division to develop +100 volts at TP-9. d. Provides current limiting. e. Voltage limiting to prevent arcing of the CRT. f. Provides a constant load on the 7 KV power supply.

P.I.	
b, c, f.	28. Select from the list below two statements that correctly describe the configuration and operation of the bleeder network. a. The bleeder network is a parallel network of resistors. b. The bleeder network operates as a voltage divider. c. A group of series resistors forms the bleeder network. d. The bleeder network operates as a voltage multiplier. e. Both parallel and series resistor combinations are used in the bleeder network.
b, c.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 8

DOWN COUNTERS (INTEGRATED FREQUENCY DIVIDER)

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-8

DOWN COUNTERS (INTEGRATED FREQUENCY DIVIDER)

In this lesson topic you will study the basic concepts of the range mark divider counter and the range gate circuits. The circuits' function, operation and output waveforms will be discussed. Circuit identification and the logic states used during operation will be shown. Upon completion of this lesson topic, a laboratory will be performed to further reinforce your understanding of the circuits function and operation.

The learning objectives for this lesson topic are as follows:

1. Select from a group of logic symbols the logic symbols that represent the one mile range mark section of the frequency divider.

2. Select from a list the statement that describes the circuit function, logic state and output of the logic element U7-C4A in the one mile range mark section.

3. Select from a list the statement that describes the circuit function, logic state and output of logic element U7-C2A in the one mile range mark section.

4. Select from a group of logic symbols the logic symbols that represent the five mile range mark section of the frequency divider.

5. Select from a list the statements that describe the circuit function, logic state and output of logic elements U3, U4, and U5 in the five mile range mark section.

6. Select from a list the statements that describe the circuit function, logic state, and output of logic element U7-D2A in the five mile range mark section.

7. Select from a group of logic symbols the logic symbols that represent the ten mile range mark section of the frequency divider.

8. Select from a list the statement that describes the circuit function, logic state and output of logic element U6 in the ten mile range mark section.

9. Select from a list the statement that describes the circuit function, logic state and output of logic element U7-E2B in the ten mile range mark section.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-8

DOWN COUNTERS (INTEGRATED FREQUENCY DIVIDER)

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job Program in Job Program Booklet.
2. Student response sheets.
    a. Job Data sheet.
    b. Answer sheet for use with test.
    c. Programmed instruction response sheets.

ENRICHMENT MATERIALS:

MIM, 15A21.

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation, consult your learning supervisor.

PROGRAMMED INSTRUCTION

DOWN COUNTERS (INTEGRATED FREQUENCY DIVIDER)

INTRODUCTION

In this lesson topic, the range marks divider-counter, range mark gate, and the range marks video pulse generator will be explained. During the detailed block diagram lesson (topic 5-3-1) the waveform analysis of the Range Marks Generator Card was covered. Circuit description, operation, logic flow, and output are divided into four (4) sections. These sections are:

1. One-mile range marks.
2. Five-mile range marks.
3. Ten-mile range marks.
4. Circuits common to all range marks sections.

1. The preceeding lesson topic on the gated 81 kHz Colpitts oscillator explained that the output of the oscillator is a sine wave with a cycle time representing one radar range mile. This signal is shaped into a train of squarewaves by shaping circuit, U2. This train of squarewaves is used by the range marks divider-

P.I.

1. (Continued)

counter and gate circuits as clock pulses for timing of the range marks.

Refer to figure 5-9 in the MIM. Since the 81 kHz square waves represent one mile range marks they are fed directly to the video pulse generator through two NAND gates U7-C4A and U7-C2A. When the 2-20/1 range position is selected the one mile range marks are routed to the video pulse generator, U8.

The logic elements used for the one-mile range marks are two NAND gates U7-________ and U7-______________.

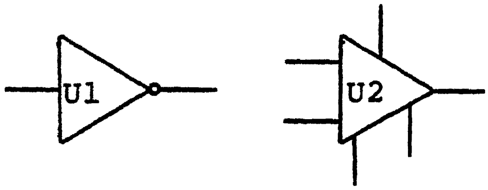
P.I.

C4A

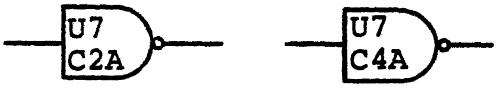
C2A

2. From the below group of logic symbols, which symbols are used in the one-mile range mark section?

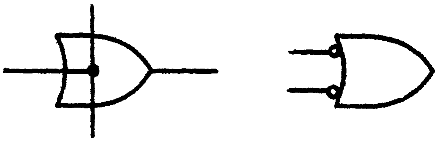
a.



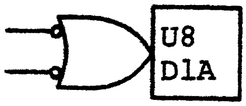
b.



c.



d.



P.I.: b.

3. Refer to figure 5-9. The input to U7-C4A consists of square waves from the pulse shaping circuit, U2. U7-C4A is a NAND gate and performs a "not" function which inverts the 81 kHz square waves. The inverted square waves appear at the output of U7-C4A (Pin 6) and are applied to U7-C2A (Pin 9).

P.I.	
	3. (Continued) The logic element U7-C4A is a NAND gate used as a ________ function to ________ the 81 kHz square waves output of U2, the pulse shaper.
not invert	4. The logic element U7-C4A is a/an a. NAND gate used to produce high outputs for high inputs in the 1 mile range marks section. b. AND gate used as a NOT function and isolates the 81 kHz square waves for the output. c. NAND gate used to perform a NOT function and invert the 81 kHz square waves in the 1 mile-range marks section. d. NOR gate used to produce high outputs for low inputs.
c.	5. The one-mile range marks section logic elements are ________ and ________, both of which are NAND gates.

P.I.	Module 5-5 Lesson Topic 5-5-8
U7-C4A U7-C2A	6. Refer to figure 5-9 in the MIM. The inverted 81 kHz square waves from U7-C4A pin 6, are applied to pin 9 of U7-C2A, another NAND gate. The other input to this NAND gate is the range marks control voltage (+5vdc) from the 2-20/1 mile contacts of the RANGE switch. This voltage enables the NAND gate, and the output is low when the input is high. The logic element U7-C2A is a ________ gate (NAND/NOR) used to produce low outputs when the input is ________ (high/low).
NAND high	7. U7-C2A is a a. NAND gate used to produce high outputs from high inputs. b. NAND gate used to produce low outputs from high inputs when enabled. c. NOR gate used to produce low outputs at all times. d. NOT circuit.

P.I.

Module 5-5
Lesson Topic 5-5-8

b.

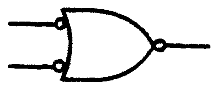
8. In the one-mile range mark section the logic element U7-C4A is a NAND gate used to perform a ________ function and ________ the 81 kHz square waves.

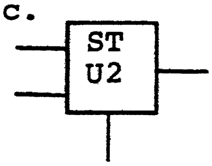
not

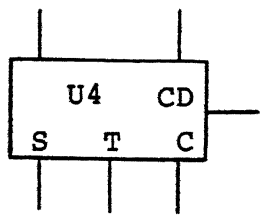
invert

9. Refer to the schematic diagram of the Range Mark Generator Card. Which two logic symbols below are used in the one-mile range marks section?

a.


b.


c.


d.


e.


f.


a,

10. Refer to figure 5-9 in the MIM. The second section of the counter-divider produces the five mile range marks.
The 81 kHz square wave train is applied from the pulse shaper, U2, to the "T" toggle input of U3. The 5-mile range marks section consists of U3, U4, U5, and U7-D2A. The circuit devices U3, U4, and U5 are J-K flip-flops and provide the counter-divider action for the generation of 5-mile range marks. When the fifth input square wave is applied to U3 and U5, the "0" (pin 9) output of U5 changes from the low to high logic state, thus generating an output representing a 5-mile range mark which can be measured at test point A3. This output of U5 is applied to pin 13 of U7-D2A, a NAND gate. When the 5-mile range marks are selected, the range control voltage (+5vdc) is applied to U7-D2A pin 12, enabling the NAND gate, whose output changes from a logic "0" to a logic "1". This allows a 5-mile range mark to be generated by the video pulse generator U8.

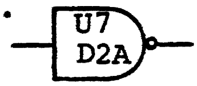
P.I.

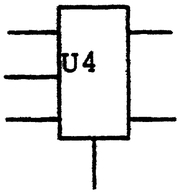
10. (Continued)

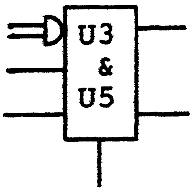
Refer to the schematic diagram of the range mark generator card. The 5-mile range mark section of the divider-counter and range mark gate consists of J-K flip-flops __________, __________, __________ and a NAND gate, __________.

U3,
U4,
U5,
U7-D2A.

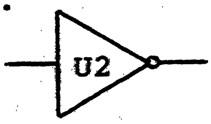
11. Which three logic symbols below are included in the 5-mile range marks section of the Range Mark Generator Card?

a.


b.


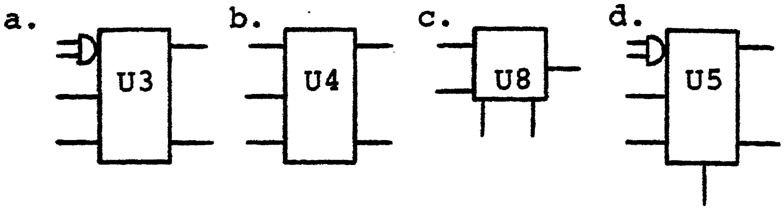
c


d.


e.


P.I.	
a, b, c.	12. The NAND gate that produces low outputs during high inputs and is enabled in the 2-20/1 position of the RANGE switch, is ___U7-D2A/U7-C2A___.
U7-C2A.	13. Refer to the schematic diagram of the Range Mark Generator Card. The logic element U7-C4A, in the one mile range mark section, is a. a NAND gate used to limit the amplitude of the 81 kHz square waves. b. an inverted OR gate used to invert the 81 kHz square waves. c. an inverted OR gate used to limit the amplitude of the 81 kHz square waves. d. a NAND gate used to perform a NOT function and to invert the 81 kHz square waves.
d.	14. Refer to the schematic diagram of the Range Mark Generator Card (A3A3). The 81 kHz square waves are applied from the shaping circuit U2 to the flip-flop U3 pin 2. When the <u>second</u> negative change occurs in the input, the flip-flop U3 will have changed its "1" output from a high to a low state triggering flip-flop U4's

P.I.	
	14. (Continued) output from low to high at pin 6. This condition will remain until the fourth negative change occurs. At this point the "O" output of U5 changes from a high to low. On the fifth input the output will reverse, generating the required output to the range gate circuit. The logic elements U3, U4, and U5 in the 5-mile range mark section are J-K _______-_______ and are used to produce one pulse for every ___________ cycles of the 81 kHz oscillator.
flip-flops five	15. Which of the following is a description, of the circuit function, logic state and output of the logic elements U3, U4, and U5? U3, U4, and U5 are a. inverter amplifiers used to invert the range marks from U2. b. J-K flip-flops to invert the range marks from U8. c. inverter amplifiers used to produce 1 output for 5 inputs from the 81 kHz oscillator. d. J-K flip-flops used as a five bit counter producing 1 output for every five inputs from the 81 kHz oscillator.

P.I.	Module 5-5 Lesson Topic 5-5-8
d.	16. In the five mile range mark section of the Range Mark Generator Card, what are the logic symbols for the three divider counters? 
a, b, d.	17. Refer to the schematic diagram of the Range Mark Generator Card. The logic element U7-C2A in the one mile range mark section is a a. NAND gate used to produce high outputs during high inputs. b. NOR gate used to produce low outputs during high inputs. c. NAND gate used to produce low outputs during high inputs. d. NOR gate used to produce high outputs during high inputs.

c.

18. Refer to the Range Mark Generator Card schematic diagram. The output pulse from U5-pin 9 is routed to the range mark gate element U7-D2A. From the schematic diagram, the circuit device is a NAND gate. The other input is a +5vdc when the RANGE switch is positioned to the 2-20/5 or 25/5 mile range. This NAND gate enables the output of the five mile range mark section and inverts the output of U5.

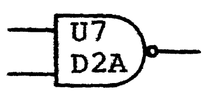
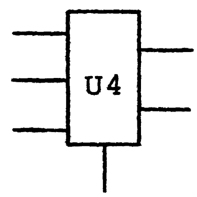
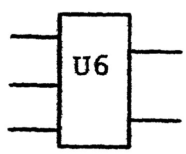
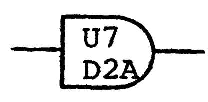
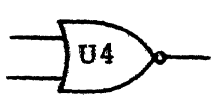
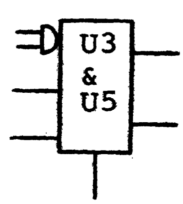
U7-D2A is a ____________ gate used to enable the output of the five mile range mark sections and __________ the output of U5.

NAND
invert

19. The logic element U7-D2A is a _____________ gate and, when enabled, __________ the output of _________________.

<table>
<tr><td>P.I.

NAND
inverts
U5</td><td>20. U3, U4, U5 are used as a five bit counter producing __________ output for every __________ inputs from the 81 kHz oscillator and consists of three ________-______.</td></tr>
<tr><td>one
five
flip-flops</td><td>21. Refer to the schematic diagram of the Range Mark Generator Card. Select the three symbols that represent the logic elements in the five mile range mark section of the frequency divider.

a. 
b. 
c. 
d. 
e. 
f. </td></tr>
</table>

P.I.

a,

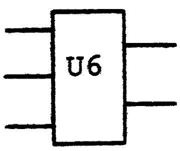
b,

f.

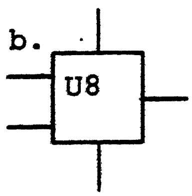
22. Refer to figure 5-9 in the MIM. The <u>ten mile</u> range mark section of the counter divider includes all of the five mile counters, U3, U4, U5, the last flip-flop, U6, and NAND gate U7-E2B. This circuitry uses the same basic operations as the five mile range mark section. The output is one pulse for every ten input cycles from the 81 kHz oscillator.

Which two of the logic symbols below are added to the five mile range mark section to form the ten mile range mark section?

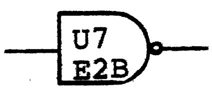
a.



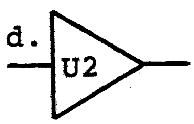
b.



c.



d.



P. I.	
a, c.	23. Refer to the schematic diagram of the Range Mark Generator Card. List the logic elements that make up the ten mile range mark divider-counter and range mark gate. ____________, ____________, ____________, ____________, and ______________________.
U3, U4, U5, U6, U7-E2B.	24. The logic element that inverts the output of U5 and enables the output of the five mile range mark section is ______________________, a NAND gate.
U7-D2A	25. Refer to figure 5-9. Select two statements that describe the circuit function, logic state, and output of logic elements U3, U4, and U5. U3, U4 and U5 are a. inverter amplifiers. b. J-K flip-flops. c. used to invert the range mark from U2. d. used as a five bit counter to produce one pulse for every five cycles of the 81 kHz oscillator.

P.I.	
b, d.	26. The logic symbol labeled U6 is another J-K flip-flop. The circuit output will change once whenever the output of the five mile range mark section changes twice. This is a 2:1 countdown that represents the ten mile range mark and requires ten inputs applied to U3 to produce one output. The logic circuit U6 employs a ______ (1:1/2:1/3:1) countdown ratio and requires ______ (2/5/10) inputs from U5 to produce one output pulse.
2:1 2	27. The logic symbol, U6, in the ten mile range mark section, is a/an a. J-K flip-flop that produces ten range marks for every one applied to U3. b. astable multivibrator that produces one range mark for every ten marks applied to U3. c. monostable multivibrator used as a 2:1 countdown device to produce one range mark for every ten marks applied to U3. d. J-K flip-flop used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5.

P.I.	
d.	28. The logic devices U3, U4, U5, U6, and U7-E2B make up the ________ ___________ range mark section of the Range Mark Generator Card.
ten mile	29. Refer to the schematic diagram of the Range Mark Generator Card. The element U7-D2A, in the five mile range mark section is, a/an _______________ gate and is a. used to enable a output from the five mile range mark section and invert the output of U5. b. used to disable the five mile range mark section to prevent the output of range marks every five miles.
NAND, a.	30. The portion of the range mark circuit that is used exclusively for ten mile range marks is U7-E2B. The inputs to this NAND gate are the output pulses from U6 and the enabling +5 vdc control voltage from the 10 mile control. The output from U7-E2B is inverted and applied to the video pulse generator. The enabling control voltage is selected by the RANGE switch on the radar Display-Indicator.

P.I.	
	30. (Continued) U7-E2B is a NAND gate used to ____________ the output of the ten mile range mark section. U7-E2B also ____________ the output from U6.
enable inverts	31. Refer to the schematic diagram of the Range Mark Generator Card. The logic symbol U7-E2B in the ten mile range mark section is a a. NAND gate used to enable the five mile range mark output to U6. b. NOR gate used to enable the ten-mile range mark section and invert the output of U6. c. NOR gate used to enable the five mile range mark section and invert the output of U6. d. NAND gate used to enable the output of the ten mile range mark section and invert the output of U6.

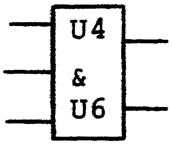
P.I.

d.

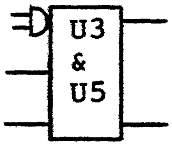
32. Refer to the schematic diagram of the Range Mark Generator Card. The logic symbol used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5 is labeled ____.

U6.

33. Refer to the schematic diagram of the Range Mark Generator Card. The three logic symbols that represent the circuits included in the ten mile range mark section are

a.


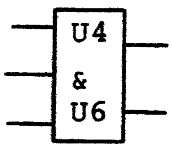
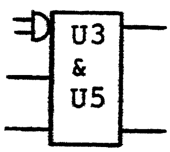
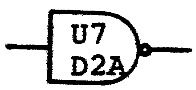
b.


c.


d.


e.


P.I.	Module 5-5 Lesson Topic 5-5-8
a, c, d.	34. The logic device in the ten mile range mark section that inverts the output of U6 and enables the output of the ten mile range mark section is ______________, a NAND gate.
U7-E2B.	35. Refer to the schematic diagram of the Range Mark Generator Card. The logic device, U6, in the ten mile range mark section is a a. monostable multivibrator that produces ten range marks for everyone applied to U3. b. J-K flip-flop used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5. c. astable multivibrator used as a 2:1 countdown device to produce one range mark for every ten miles. d. J-K flip-flop producing 10 range marks for each input.

P.I.	
d.	32. Refer to the schematic diagram of the Range Mark Generator Card. The logic symbol used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5 is labeled ____.
U6.	33. Refer to the schematic diagram of the Range Mark Generator Card. The three logic symbols that represent the circuits included in the ten mile range mark section are a.  b.  c.  d.  e. 

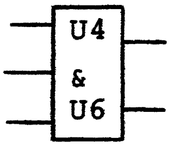
P.I.	Module 5-5 Lesson Topic 5-5-8
a, c, d.	34. The logic device in the ten mile range mark section that inverts the output of U6 and enables the output of the ten mile range mark section is ______________, a NAND gate.
U7-E2B.	35. Refer to the schematic diagram of the Range Mark Generator Card. The logic device, U6, in the ten mile range mark section is a a. monostable multivibrator that produces ten range marks for everyone applied to U3. b. J-K flip-flop used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5. c. astable multivibrator used as a 2:1 countdown device to produce one range mark for every ten miles. d. J-K flip-flop producing 10 range marks for each input.

d.

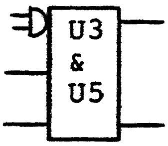
32. Refer to the schematic diagram of the Range Mark Generator Card. The logic symbol used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5 is labeled ____.

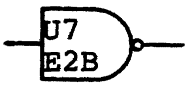
U6.

33. Refer to the schematic diagram of the Range Mark Generator Card. The three logic symbols that represent the circuits included in the ten mile range mark section are

a.


b.


c.


d.


e.


P.I.	
a, c, d.	34. The logic device in the ten mile range mark section that inverts the output of U6 and enables the output of the ten mile range mark section is ______________, a NAND gate.
U7-E2B.	35. Refer to the schematic diagram of the Range Mark Generator Card. The logic device, U6, in the ten mile range mark section is a a. monostable multivibrator that produces ten range marks for everyone applied to U3. b. J-K flip-flop used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5. c. astable multivibrator used as a 2:1 countdown device to produce one range mark for every ten miles. d. J-K flip-flop producing 10 range marks for each input.

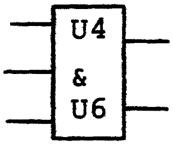
P.I.

d.

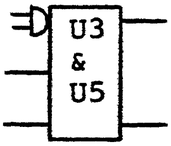
32. Refer to the schematic diagram of the Range Mark Generator Card. The logic symbol used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5 is labeled ____.

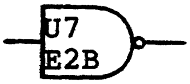
U6.

33. Refer to the schematic diagram of the Range Mark Generator Card. The three logic symbols that represent the circuits included in the ten mile range mark section are

a.


b.


c.


d.


e.


P.I.	
a, c, d.	34. The logic device in the ten mile range mark section that inverts the output of U6 and enables the output of the ten mile range mark section is _______________, a NAND gate.
U7-E2B.	35. Refer to the schematic diagram of the Range Mark Generator Card. The logic device, U6, in the ten mile range mark section is a a. monostable multivibrator that produces ten range marks for everyone applied to U3. b. J-K flip-flop used as a 2:1 countdown device to produce one range mark for every two 5-mile range marks applied from U5. c. astable multivibrator used as a 2:1 countdown device to produce one range mark for every ten miles. d. J-K flip-flop producing 10 range marks for each input.

P.I.	
b.	36. Refer to the schematic diagram for the range mark generator card. Logic element U7-E2B in the ten mile range mark section is a a. "NAND" gate used to enable the five mile range mark section and invert the output of U6. b. "NOR" gate used to enable the five mile range mark section and invert the output of U6. c. "NAND" gate used to enable the ten mile range mark section and invert the output of U6. d. "NOR" gate used to enable the ten mile range mark section and invert the output of U6.
c.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 9

MONOSTABLE MULTIVIBRATOR

NOVEMBER 1975

OVERVIEW

LESSON TOPIC 5-5-9

MONOSTABLE MULTIVIBRATOR

In this lesson topic you will study the Monostable Multivibrator on the Range Mark Generator Card (A3A3). You should thoroughly understand the circuit configuration, function, voltage requirement, logic relationship, and output waveform. Upon the completion of the lesson topic, a laboratory exercise will further aid your understanding of the monostable multivibrator by observing the circuit in operation within an airborne search radar system.

The learning objectives for this lesson topic are as follows:

1. Select from a list of logic symbols the logic symbol for the monostable multivibrator in the range mark generator circuit.

2. Select from a list the external circuit components used with the monostable multivibrator, U8.

3. Select from a list of statements, the statement that describes the function of the integrated circuit monostable multivibrator.

4. Select from a list the statement that explains the circuit function of the external circuit components of the monostable multivibrator circuit.

5. Select from a list the statement that describes the voltage required to trigger the monostable multivibrator.

6. Select from a list the statement that describes the voltage-to-logic relationship in the monostable multivibrator.

7. Select from a list the statement that describes how the output of the monostable multivibrator is affected during high-to-low changes in the input.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-9

MONOSTABLE MULTIVIBRATOR

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job Program in Job Program Booklet.
2. Student response sheets.
    a. Job data sheet.
    b. Answer sheet for use with test.
    c. Programmed instruction response sheets.

ENRICHMENT MATERIALS (topic references):

1. Maintenance Instruction Manual, 15A21.
2. Aviation Electronics Technician 3 & 2, NAVPERS 10317-D, Chapter 10.

All the resources listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

MONOSTABLE MULTIVIBRATOR

INTRODUCTION

In this lesson topic you will be taught the circuit configuration, function, operation, voltage requirements, logic relationships and output waveform of the Video Pulse Generator A3A3U8.

1. The video pulse generator circuit on the Range Marks Generator Card is used to generate the one, five and ten mile range mark video pulses. The duration of the individual pulses is one microsecond. These pulses are applied to the radar display-indicator and appear as rings on the CRT as the sweep rotates.

   A monostable multivibrator, which consists of an integrated circuit, is used to develop the range mark video pulses.

   The symbol for the integrated circuit multivibrator used in the Range Mark Generator Card is illustrated in figure 1.

P.I.

1. (Continued)

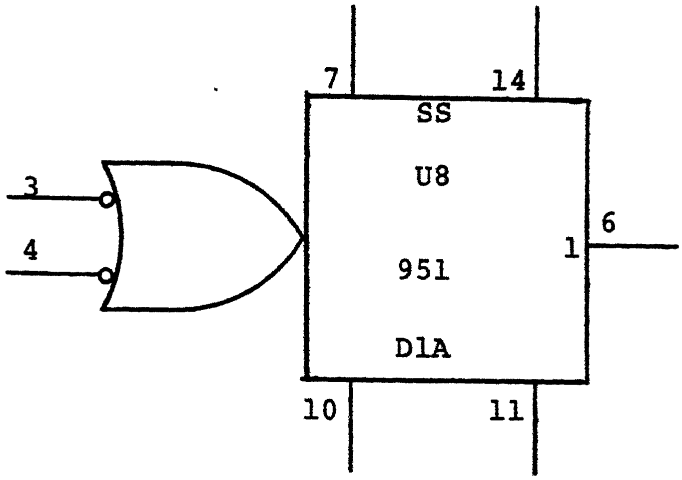


FIGURE 1

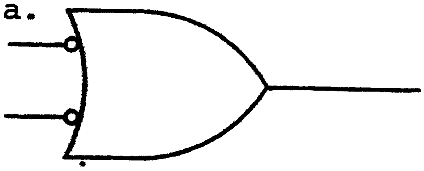
The (SS) represents the single-swing function of the circuit. The reference designator for this integrated circuit is A3A3U8. Also located on the symbol is 951D1A which identifies the specific type of integrated circuit. The numbers adjacent to the external lines identify the external connections.

Refer to the Range Marks Generator Card schematic diagram in the MIM. (Figure 5-9).

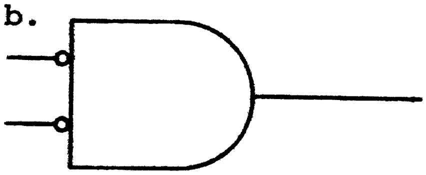
1. (Continued)

Select the symbol from the below list that represents the monostable multivibrator.

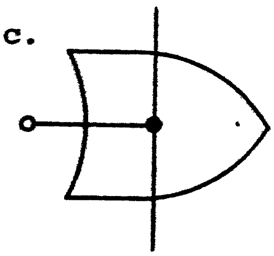
a.



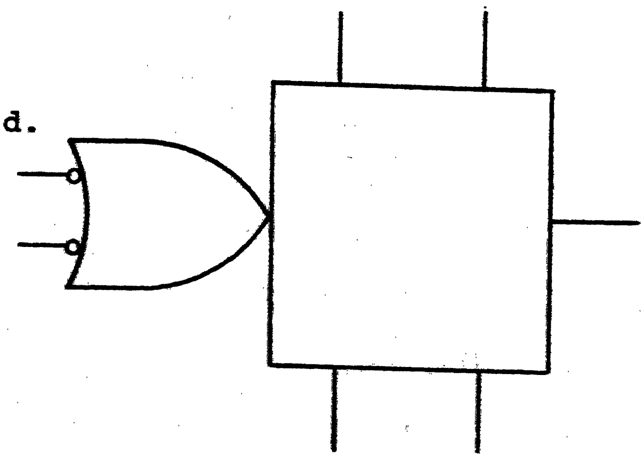
b.



c.



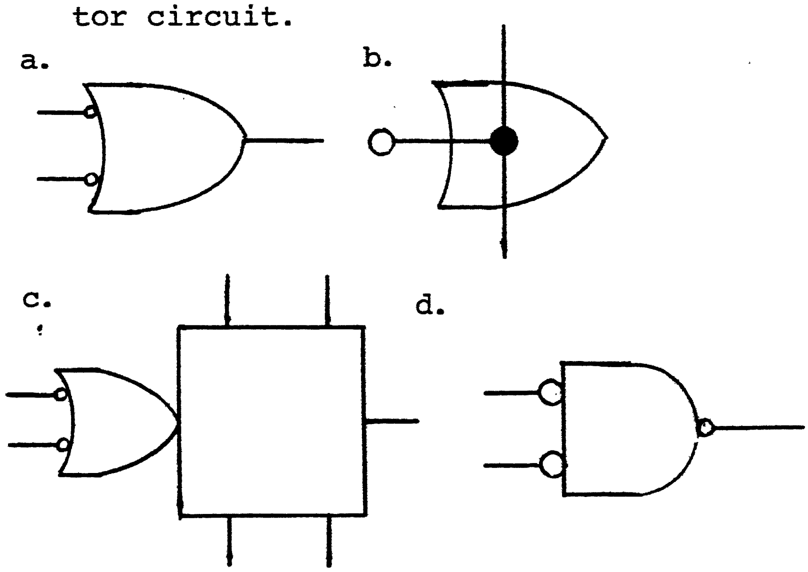
d.



P.I.

d.

2. Refer to figure 5-9. Select the symbol that represents the monostable multivibrator circuit.



---

c.

3. Refer to the schematic diagram of the Range Marks Generator Card. The components used with the monostable multivibrator, U8, are two capacitors C9 and C10. The circuit function of these components will be explained later within this lesson topic.

The external components used with the integrated circuit multivibrator, U8, are ________________ and ____________________.

C9
C10

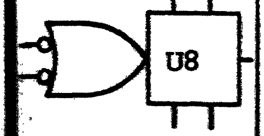
4. Which external circuit components are used with the monostable multivibrator?

a. C10.
b. U8.
c. U7.
d. C9.

a,

d.

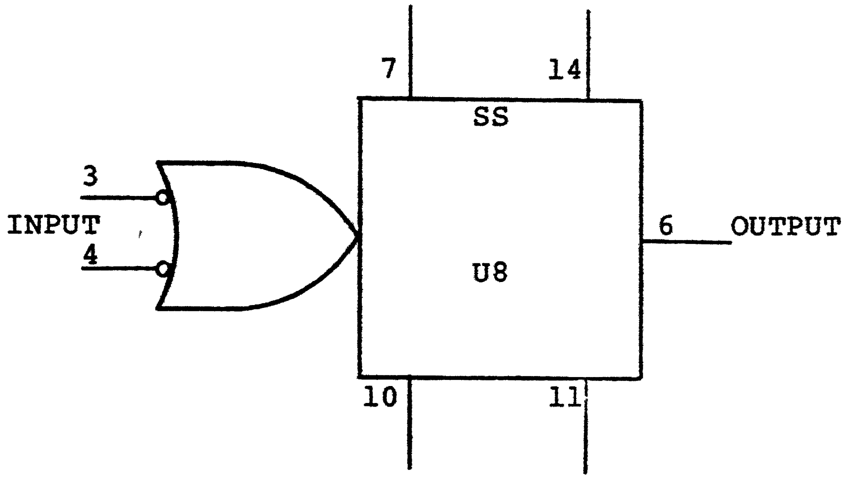
5. Draw the logic symbol for the integrated circuit multivibrator of the range marks generator circuit.



6. The inputs to U8 are applied to pins 3 and 4 from the 1, 5, or 10 mile range marks countdown circuits. The function of U8 is to convert the pulses from the countdown circuits to usable range mark pulses.

6. (Continued)

The synchrogram in figure 2 depicts the input and output waveforms of the mono-stable multivibrator.



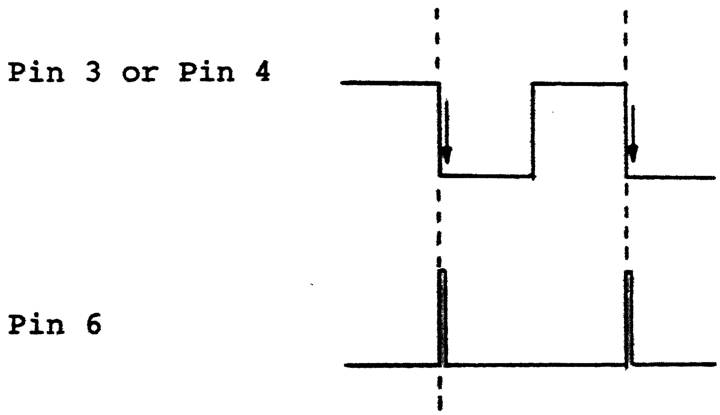


FIGURE 2

P.I.	
	6. (Continued) The monostable multivibrator produces a __________ output pulse (a range mark) whenever the input at pin 3 or pin 4 goes in a ______________ direction.
positive negative	7. Select the correct description of the input-output waveforms relationships. a. The output pulses occur at half the frequency of the input. b. The output is a positive pulse each time the input changes from high to low. c. The output is positive each time the input changes from low to high.
b.	8. Refer to the Range Marks Generator schematic diagram. The monostable multivibrator consists of ___________, ___________, and ______________.

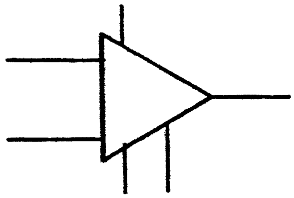
P.I.

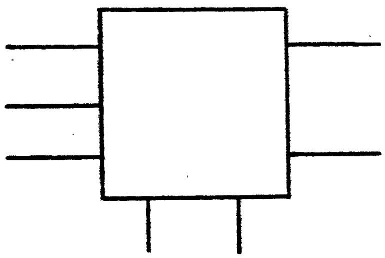
U8,

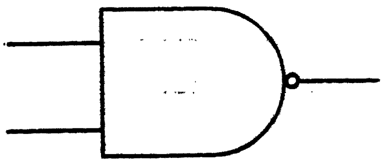
C9,

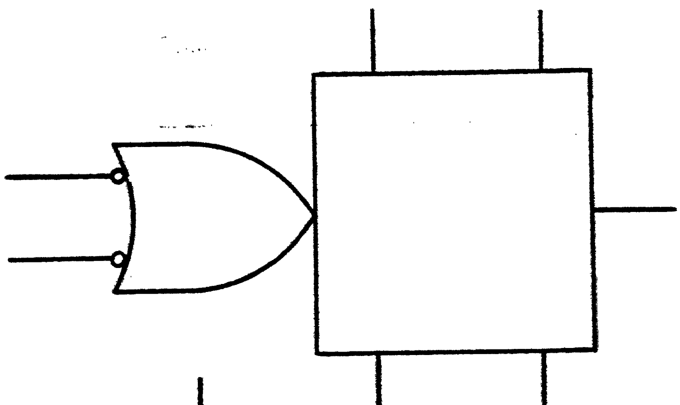
C10.

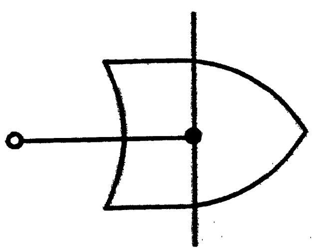
9. Which logic symbol represents the monostable multivibrator in the range mark generator circuit?

a. 

b. 

c. 

d. 

e. 

P.I.	
d.	10. The capacitors C9 & C10 are used in the monostable multivibrator external circuitry and aid the multivibrator in the development of the correct pulse output from the Video Pulse Generator. Capacitor C9 is a filter capacitor connected from +5vdc to ground and is used to filter out unwanted fluctuations that may exist in the +5vdc power supply voltage. Capacitor C10 is used to determine the exact duration of the output pulse width and is connected to provide wave-shaping of the output pulse. Capacitor C9 provides ____________ of any possible ripple from the +5vdc supply and C10 provides wave-shaping action to determine the output _________ ____________.

P.I.	Module 5-5 Lesson Topic 5-5-9
filtering pulse width	11. The functions performed by C9 and C10 in the monostable multivibrator are a. C9 is used to filter out ac ripple on the input pulses. b. C10 is used for wave-shaping to determine the output pulse width. c. C9 is used to filter out any ripple in the +5vdc power supply voltage. d. C10 is used as an integrating capacitor to waveshape the input pulses.
b, c.	12. A monostable multivibrator will develop an output frequency equal to the input frequency. U8 will produce a positive pulse output when the input at (pin 3 or 4) goes in a ____________________ direction.
negative	13. Select the external circuit components used with the monostable multivibrator. a. U7. b. U8. c. C9. d. C10.

P.I.	
c, d.	14. The preceeding lesson topic, 5-5-8, explained that the output of the range gate circuit, U7, consists of positive pulses. The multivibrator uses the trailing edge, (when the pulse goes from the high state to the low state), as a trigger pulse. This voltage change causes the monostable multivibrator to cycle once for each output from the selected range gate circuitry. The voltage change required to trigger the monostable multivibrator is a ______________ change. low-to-high/high-to-low
high-to-low	15. The monostable multivibrator requires what input voltage change to trigger each cycle of operation? a. Constant high voltage. b. High-to-low changing voltage. c. Zero volts. d. Low-to-high changing voltage.

P.I.	Module 5-5 Lesson Topic 5-5-9
b.	16. Refer to the schematic diagram of the Range Marks Generator Card. The function of the externally connected capacitors, C9 and C10, of the monostable multivibrator are: a. C9 is a ______________ capacitor. b. C10 is used for wave-shaping to determine the output __________ width.
a. filter b. pulse	17. Which statement correctly describes the relationship of input to output of the integrated circuit monostable multivibrator, U8? a. U8 will produce an output positive pulse each time the input to pin 3 or 4 changes from high to low. b. U8 will produce an output positive pulse each time the input to pin 3 or 4 changes from low to high. c. The output pulses occur at half the frequency of the input. d. The output pulses are independent of the frequency of the input.
a.	18. The high-to-low voltage change that triggers the monostable multivibrator can also be referred to a logic state requirement. As taught in the unit of instruction on computers, any voltage change has a definite

P.I.	 18. (Continued) relationship to a logic state. The type of logic employed by the monostable multivibrator is positive logic. The relationship of the voltage-to-logic is that the high state represents a positive voltage and the low state represents zero volts. In the monostable multivibrator the high logic state represents a ________ voltage and the low logic state is ________ volts.
positive zero	19. Which statement describes the voltage-to-logic relationship in the monostable multivibrator, U8. a. Zero volts is high and a positive voltage is low. b. Positive voltage is low and a negative voltage is high. c. Negative voltage is a low and zero volts is high. d. Negative voltage is high and zero volts is low. e. Positive voltage is high and zero volts is low.

P.I.	Module 5-5 Lesson Topic 5-5-9
e.	20. The voltage change required to trigger the monostable multivibrator is a ________-__________-___________ changing voltage.
high-to-low	21. The two statements that describe the function of the external circuit components of the monostable multivibrator are: a. C10 is used as an integrating capacitor to waveshape the input pulses. b. C9 is used to filter out fluctuations in the +5vdc power supply voltage. c. C10 is used to block dc voltages from pin 11 on U8. d. C9 is used to filter out ac ripple from the input pulses. e. C10 is used for wave-shaping to determine the output pulse width.
b, e.	22. When the input to the monostable multivibrator, U8, makes a high-to-low voltage change, U8 will produce an output positive pulse of 1 μsec in duration. C10 aids in the production of 1 μsec pulses by wave-shaping. The output pulses must be 1 μsec in duration in order to be visible on the indicator.

P.I.	
	22. (Continued) When the input voltage to U8 goes in a negative direction, the multivibrator produces an output positive pulse ________ in duration.
1 μsec	23. When the input to the monostable multivibrator switches from high-to-low, the effect seen in the output of the multivibrator is a. sinewave oscillations. b. a change of high-to-low and a return to high. c. the output does not change. d. a positive output pulse, 1 μsec in duration.
d.	24. The voltage-to-logic relationship in the monostable multivibrator is that a positive voltage is ____________ and zero volts is ________________.

P.I.	
high low	25. The voltage change needed to trigger the monostable multivibrator is a a. constant low voltage. b. low-to-high changing voltage. c. constant high voltage. d. high-to-low changing voltage.
d.	26. The input to U8 must go ____________ in order for U8 to produce an output pulse.
low	27. Select the statement that describes the voltage-to-logic relationship in the monostable multivibrator. a. Negative voltage is a low and zero voltage is a high. b. Negative voltage is a high and zero voltage is a low. c. Positive voltage is a high and zero voltage is a low. d. Negative voltage is a low and positive voltage is a high. e. Zero voltage is a high and positive voltage is a low.

P.I.	
c.	28. Select the statement that describes how a high-to-low change in the input affects the output of the monostable multivibrator. a. During the high-to-low change in the input the output does not change. b. A high-to-low change at the input causes the output to go from low-to-high and remain there until the next low-to-high change. c. A change of high-to-low and a return to high occurs on the output during high-to-low changes at the input. d. During the input change the output is a sinewave oscillation. e. The output is a positive pulse, 1 μsec in duration.
e.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 10

ISOLATING MALFUNCTIONING PARTS IN THE SYNCHRONIZER-DISPLAY INDICATOR UNITS

DECEMBER 1976

OVERVIEW

LESSON TOPIC 5-5-10

ISOLATING MALFUNCTIONING PARTS IN THE SYNCHRONIZER-DISPLAY INDICATOR UNITS

In this lesson topic you will perform troubleshooting to a defective stage/part in the display indicator and synchronizer units. The OMA and IMA levels of maintenance will be performed and documented on the MAF and the trouble-shooting worksheet for the airborne search radar system trainer.

The learning objective for this lesson topic is as follows:

Given the radar MIM and required test equipment, trouble-shoot a malfunctioning radar synchronizer and display indicator to a defective stage/part as specified on the troubleshooting worksheet.

NOTE: The objective in this lesson topic must be accomplished with 90 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-10

ISOLATING MALFUNCTIONING PARTS IN THE SYNCHRONIZER-DISPLAY INDICATOR UNITS

There are no written lesson topic presentations for this lesson topic. You may review any of the resources in lesson topic 5-5-1 through lesson topic 5-5-9 before going to lab if you desire.

MATERIAL REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

1. Job Program in Job Program Booklet.
2. Student response sheets.
   a. Troubleshooting worksheet for airborne search radar system trainer.

ENRICHMENT MATERIALS:

1. MIM, 15A21.
2. Aviation Electronics Technician 3 & 2, NAVPERS 10317-D, Chapter 13, Electronic Maintenance.

AVIONICS TECHNICIAN COURSE, CLASS A1

UNIT 5

MODULE 5

LESSON TOPIC 11

PROPER HANDING AND DISPOSAL OF CATHODE RAY TUBES

DECEMBER 1976

OVERVIEW

LESSON TOPIC 5-5-11

PROPER HANDLING AND DISPOSAL OF CATHODE RAY TUBES

In this lesson you will learn the approved maintenance procedures for handling cathode ray tubes. Great emphasis will be placed on safe handling and disposal of these potentially dangerous devices.

The learning objectives for this lesson topic are as follows:

1. Select, from a list, the three safety precautions an individual should adhere to when disposing of a cathode ray tube.

2. Select, from a list, the four safety precautions related to the care of a cathode ray tube.

3. Select, from a list, the statement that correctly describes the proper method to be used for removal of a cathode ray tube.

4. Select, from a list, three statements that describe the correct procedure for rendering a cathode ray tube harmless from implosion before disposal.

NOTE: All objectives in this lesson topic must be accomplished with 100 percent accuracy, unless otherwise stated.

Prior to beginning this lesson topic, carefully review the "List of Study Resources". Keep in mind that your learning supervisor can be your most valuable learning resource. Always feel free to consult with him if you have problems or questions.

LIST OF STUDY RESOURCES

LESSON TOPIC 5-5-11

PROPER HANDLING AND DISPOSAL OF CATHODE RAY TUBES

To learn the material in this lesson topic, you may choose, according to your experience and preferences, any or all of the following written lesson topic presentations.

WRITTEN LESSON TOPIC PRESENTATIONS IN MODULE BOOKLET:

1. Lesson topic summary.
2. Programmed instruction form of lesson topic.
3. Narrative form of lesson topic.
4. Lesson topic progress check.

ADDITIONAL MATERIALS REQUIRED FOR SUCCESSFUL COMPLETION OF LESSON TOPIC:

Student Response Sheets.
- a. Answer sheet for use with test.
- b. Programmed instruction response sheets.

ENRICHMENT MATERIALS:

1. NAVPERS 10376-C, Tradevman 3 & 2, Chapter 15, p. 406.
2. NAVPERS 10087-B, Basic Electronics, Chapter 17.
3. NAVPERS 10317-A, Aviation Electronics Technician 3 & 2, Chapter 2.

All the resouces listed above are available and may be used as you see fit. Your learning supervisor represents a most valuable learning resource. Use him when you need help. It is not necessary to use all the resources to achieve the learning objectives for the lesson topic. The lesson topic progress check is your means of determining when you have achieved the objectives. The progress check may be taken at any time and is graded by you. If you fail to achieve any objective at the lesson topic level, you will plan and accomplish your own remediation. If you need help in remediation planning, consult your learning supervisor.

PROGRAMMED INSTRUCTION

PROPER HANDLING AND DISPOSAL OF CATHODE RAY TUBES

INTRODUCTION

In this lesson topic, safety habits of a general nature applicable to any CRT are discussed. Particular precautions to be observed when working with a specific type of CRT are covered in the appropriate maintenance manual for that equipment.

The transportation, removal, or installation of a cathode-ray tube (CRT) is the responsibility of the technician working in an avionics rate. The CRT is not considered dangerous if handled properly, but if struck, scratched, dropped, or handled improperly in any way, it may become an instrument that could cause severe injury or death. Safety precautions to be observed when working with a CRT can be divided into two categories. One category concerns safety habits of the individual working around a CRT. The second category deals with proper safety habits when caring for the CRT.

The primary purpose of any safety education program is to prevent personnel injury or material damage. For any safety program to be effective, all affected personnel should be aware of the potential hazards and observe all safety precautions during the maintenance effort.

P.I.

1. The cathode-ray tube inherited a characteristic of its smaller brother, the vacuum tube. This characteristic is called IMPLOSION. A high vacuum exists inside the envelope of a CRT, therefore the envelope is under great stress from the atmospheric pressure. If this force becomes too great, the envelope will collapse. This is implosion. The result is flying glass and other particles propelled in such a manner to cause severe injury. Because of the hazard of implosion, the individual handling a CRT should observe the following safety precautions:

   a. Wear protective goggles and gloves.

   b. Never stand directly in front of the tube.

   c. Prevent the chemical coating on the inside face of the CRT from coming in contact with the hands or skin during disposal.

   The first two precautions will help to prevent injury if implosion occurs. The third precaution will prevent injury to personnel handling the CRT during the

P.I.	 1. (Continued) disposal process. The chemical coating is poisonous if absorbed into the blood stream. In addition to these stated safety precautions, COMMON SENSE by the individual is still the most important factor in safety on the job. Always, if in doubt, ask your supervisor. The collapse of the glass envelope of the cathode-ray tube caused by atmospheric pressure, is called ________________. implosion/explosion
implosion	2. Select the three safety precautions an individual should observe when disposing of a cathode-ray tube. a. Wear protective goggles and gloves. b. Stand in front of the tube to minimize danger of implosion. c. Stand on a rubber mat while handling the tube. d. Prevent the chemical coating on the inside face of the CRT from coming in contact with the hands or the skin. e. Never stand directly in front of the tube. f. Wear ear plugs to minimize noise in the event of implosion.

P.I.

a, d, e.

3. The danger of the implosion of a CRT presents a hazard to maintenance personnel.

To prevent implosion when handling, installing, or removing a CRT, the technician must use extreme care to avoid any contact of the tube with sharp or hard objects. Carrying a CRT will require the use of both hands on the face of the CRT. Never carry a CRT by its neck with one hand, because the neck is a weak part of the tube. Most CRT's are fastened in the equipment by a set of clamps. Excessive torque should not be used when tightening the clamp as the delicate shell of the CRT might break. Use only moderate pressure to secure the clamps. Any failure to observe these safety precautions concerning the care of the CRT could lead to personnel injury.

Safety precautions must be observed by avionics personnel in handling cathode-ray tubes to prevent ________________ from occurring.

P.I.	
implosion	4. Which four of the following safety precautions are related to the care of the cathode-ray tube? a. Coat the face of the tube with the proper chemical to prevent implosion. b. Never carry or hold the tube by its neck. c. Hold or carry the tube with both hands. d. Break the vacuum seal prior to installation of the cathode-ray tube. e. Use only moderate pressure when securing the clamps to hold the CRT in place. f. Aviod any contact of the tube with sharp or hard objects.
b, c, e, f.	5. Complete the following statements concerning the precautions an individual should observe when handling or disposing of a CRT. a. Wear protective ______________ and ______________. b. Never stand directly in __________ of the tube. c. Prevent the __________ ______________ on the inside face of the CRT from coming in contact with the ________ or the ______________________.

P.I.	
a. glasses gloves b. front c. chemical coating hands skin	6. If the CRT in a radar indicator or television becomes defective, the avionics technician will be required to remove it. The exact procedure will vary with the type of equipment. Again, always check the appropriate maintenance manual before making any attempt to remove a CRT. One precaution to observe when removing a CRT after all electrical and mechanical connections have been removed is to <u>hold</u> the CRT <u>with both hands on the face of the tube</u> and gently slide the CRT from the socket. When all electrical and mechanical connections have been removed, hold the CRT with ____________ hand/s on the ________________ one/both face/neck of the tube and gently slide the CRT from the socket.

P.I.	Module 5-5 Lesson Topic 5-5-11
both face	7. The proper method used for CRT removal is to ________. a. clamp a holder to the neck of the CRT and remove the tube quickly. b. hold the CRT with one hand on the neck of the tube and gently remove the tube from the socket. c. hold the CRT with both hands on the face of the tube and gently slide the CRT from the socket. d. hold the CRT with both hands on the neck of the tube and gently slide the tube from the socket.
c.	8. When handling a CRT, safety precautions must be observed. Lack of safety precautions could cause damage to the CRT or result in personnel injury. List four safety precautions related to the care of a CRT. (a) (b) (c) (d)

8. (Continued)

ANSWERS

Avoid any contact of the tube with sharp or hard objects.

Hold or carry the tube with both hands.

Use only moderate pressure when securing the clamps to hold the CRT in place.

Never carry or hold the tube by its neck.

9. Select the three safety precautions an individual should observe when disposing of a cathode-ray tube.

   a. Wear protective glasses and gloves.

   b. Wear ear plugs to minimize noise in the event of implosion.

   c. Stand in front of the tube to minimize the danger of implosion.

   d. Prevent the chemical coating on the inside face of the CRT from coming in contact with the hands or the skin.

   e. Never stand directly in front of the tube.

   f. Stand on a rubber mat while handling the tube.

P.I.	
a, d, e.	10. When a defective cathode-ray tube (CRT) has been removed from a radar indicator or television, it becomes necessary to discard it. It is not a simple matter of throwing the CRT into a trash receptacle. The danger of implosion must be removed before disposal is completed. The first step is to place the defective CRT, face down, into an empty CRT carton. Second, carefully break off the locating pin on the tube base. See figure 1. The last step is to break the vacuum seal of the CRT with a screw-driver or a pair of pliers. Once the vacuum seal has been broken, the danger of implosion is removed, but all other hazards still remain. To complete the disposal of

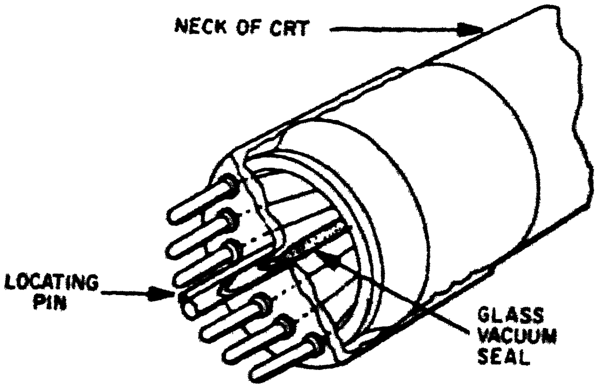


FIGURE 1

P.I.	 10. (Continued) a defective CRT, check the instructions of the local station or ship. The danger of ____________ must be removed before the disposal of a CRT. implosion/explosion
implosion	11. Select three of the following statements describing the procedure, in the correct order, for removing the danger of implosion from a CRT before disposal? a. Place the defective CRT, face up, in an empty container. b. Place the defective CRT, face down, in an empty CRT carton. c. Break the vacuum seal of the CRT with a screwdriver or a pair of pliers. d. Remove the chemical coating from the CRT. e. Carefully break off the locating pin on the tube base.

P.I.	Module 5-5 Lesson Topic 5-5-11
b, e, c.	12. Removing a CRT can be a dangerous task if not completed properly. The first two steps are to consult a maintenance manual and to remove electrical and mechanical connections, in that order. State the proper method to use when physically removing a CRT from its unit. ____ ____ ____.

P.I.	
Hold with both hands on the face of the CRT and gently slide the tube from the socket.	13. Select four safety precautions that are related to the care of cathode-ray tubes. a. Hold or carry the tube by its neck only. b. Break the vacuum seal prior to installation of the cathode-ray tube. c. Never carry or hold the tube by its neck. d. Coat the face of the tube with the proper chemical to prevent implosion. e. Hold or carry the tube with both hands. f. Avoid any contact of the tube with sharp or hard objects. g. Use only moderate pressure when securing the clamps to hold the tube in place.
c, e, f, g.	14. The danger of the implosion of a CRT must be removed before the CRT can be disposed of in accordance with the instructions of the local station or ship. List the three steps, in the proper order, to remove the danger of implosion from a CRT before disposal. a. b. c.

P.I.	Module 5-5 Lesson Topic 5-5-11 14. (Continued) ANSWERS
	a. Place the defective CRT, face down, in an empty CRT carton. b. Carefully break off the locating pin on the tube base. c. Break the vacuum seal of the CRT with a screwdriver or a pair of pliers.
	15. Select the statement that describes the proper method to use when removing a CRT. a. Hold the CRT with both hands on the neck of the tube and gently slide the CRT from the socket. b. Clamp a holder to the neck of the CRT, and remove the tube quickly. c. Hold the CRT with only one hand on the neck of the tube and gently slide the CRT from the socket. d. Hold the CRT with both hands on the face of the tube and gently slide the tube from the socket.

P.I.	
d.	16. Select three statements, in the proper order, that correctly describe the procedure for removing the danger of implosion from a CRT before disposal. a. Break the vacuum seal of the CRT with a screwdriver or a pair of pliers. b. Place the defective CRT, face up, in an empty container. c. Carefully break off the locating pin on the tube base. d. Place the defective CRT tube, face down, in an empty CRT carton.
d, c, a.	At this point, you may take the lesson topic progress check. You may find it beneficial to review the objectives for this lesson topic. If you answer all self-test items correctly, go on to the next lesson topic. If not, select and use another medium of instruction, narrative, or consultation with the learning supervisor, until you can answer all self-test items on the progress check correctly (achieve lesson topic learning objectives) and then proceed to the next lesson topic.